

Compal Confidential

EH7LW/EH5LW/FH5TW/EH7LC/EH5LC

UMA MB Schematic Document

LA-H792P

Rev: 2.0
2019.05.29

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Cover Sheet	
2018/12/27		2019/12/27		Document Number	
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HDMI Conn.



page 29

DDI2
HDMI x 4 lanes

eDP



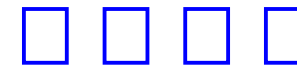
page 28

eDP

DDI

Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16



page 19

260pin DDR4-SO-DIMM X1



page 20

Memory BUS
Dual Channel

1.2V DDR4 2400

Intel Whiskey lake U
Intel Comet lake U

Processor

Cannon Lake PCH-LP

46x24 mm

15W

1528pin BGA
page 07~18

WHL-U 4+2
WHL-U 2+2

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022

page 36

Int.KBD



page 37

Touch Pad

PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)



page 37

USB 3.0
conn x1
USB3 port 1
USB2 port 1



page 35

USB 2.0
conn x2
USB2 port2 (MB)
USB2 port4(SUB)



page 35

CMOS
Camera
USB2 port 7



page 28

Card Reader
RTS5140
Reserved

USB2 port 6(SUB)

Finger
Printer
USB2 port 5

page 28

USBx8 48MHz

HD Audio

3.3V 24MHz

HDA Codec
ALC255

page 32

Touch
Screen

USB2 port 3
page 28

Int. Speaker

page 32

Int. DMIC
on Camera

page 28

UAI

page 35



page 32

NGFF
WLAN

support CNVi
USB2 port 10



PCIe 1.0
2.5GT/s
port 6
page 31

LAN(GbE)
Realtek 8111H

page 30

RJ45 conn.



SATA HDD
Conn.



page 33

SATA ODD
Conn.

SATA Gen 3
6.0 Gb/s
(SATA2)

PCIe 3.0 x4
8GT/s
Port 9-12

Flexible IO

Base-U PCIe 3.0x2 (CML)

SATA Gen 3
6.0 Gb/s
port 0
(SATA0)

SATA Gen 1
1.5 Gb/s
port 1
(SATA1A)

Sub Board

LS-H802P
HDD/B
page 26

LS-H783P
LID/B
page 31

LS-H781P
IO/B
page 31

LS-H784P
ODD/B
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Fan Control

page 32

RTC CKT.

page 15

Power On/Off CKT.

page 30

DC/DC Interface CKT.

page 33

Power Circuit DC/DC

page 34~43

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Vcc	3.3V +/- 5%					
Ra	100K +/- 1%					
Board ID	Rb	V _{BI} D min	V _{BI} D typ	V _{BI} D max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1 (EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	0.2 (DVT)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	0.3 (PVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.0 (PreMP)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CODEC	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
CNVi /BT PCM Select	CNVI@/PCM@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
TPM	TPM@
Finger Print	FP@/FPFMC@
Finger print power	FP3V@/FP5V@
UMA or DGPU	UMA@/VGA@
CPU Select	WHL@/CML@
SATA/ODD select	RD@/NRD@/ODD@
USB charger	CHG@

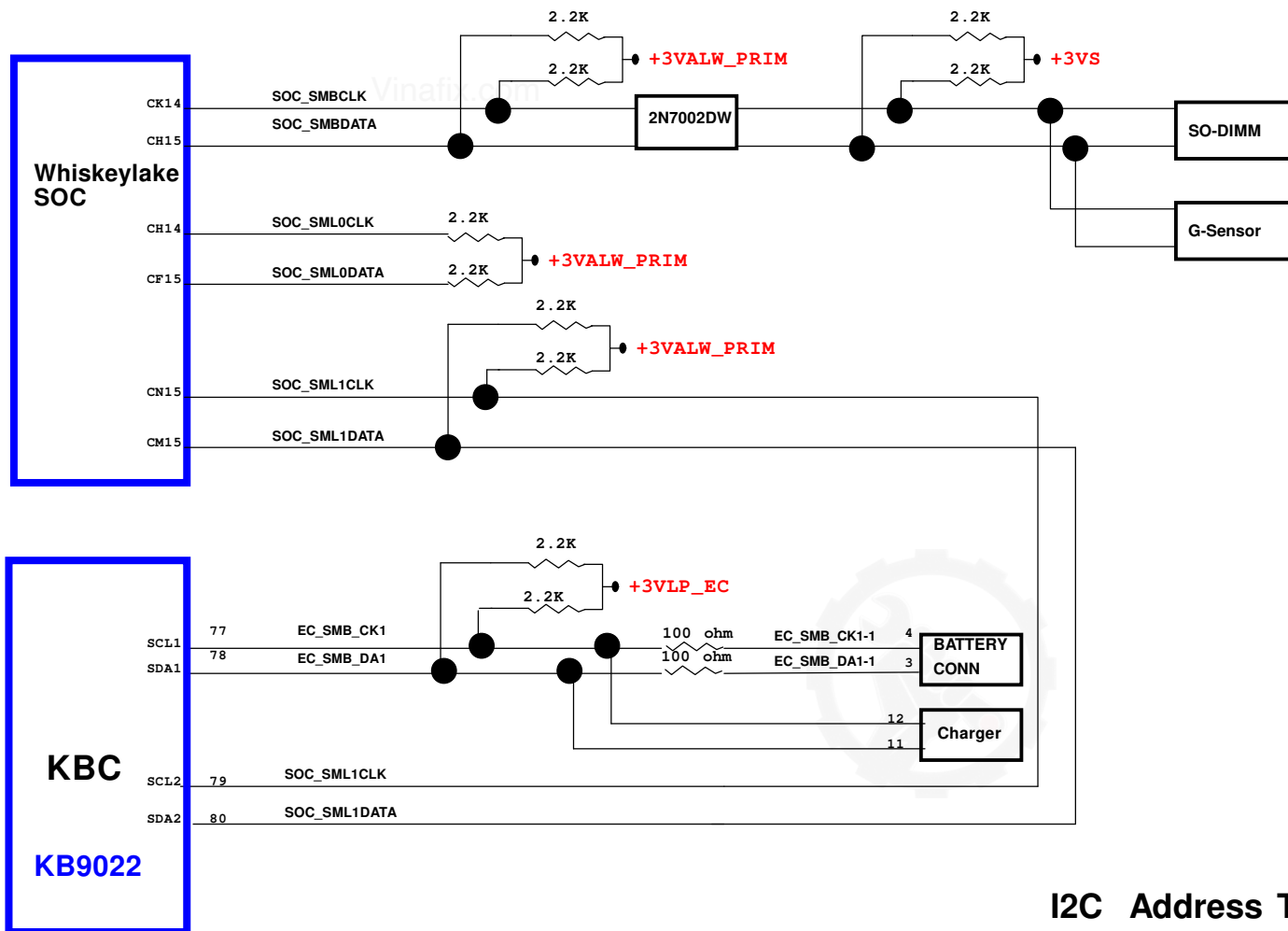
BOM Option Table	
Item	BOM Structure
MB Stage	EVT@/DVT@/PVT@/MP@
G Sensor	GSEN@
For over 3 cell battery	3S@
MD BOM Select	NOX76@/X76DSAM@/ X76DMIC@/X76DHYN@/
Memory related	SPD@/DDP@/MEM@
CPU C10 support	C10@
BOM select	15DIS@/15@/

[illegible]

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.05VALW_PRIM	+1.05V Always power rail	ON	ON	ON*1
+1.05V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.05VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VSDGPU	+1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON*2	OFF	OFF

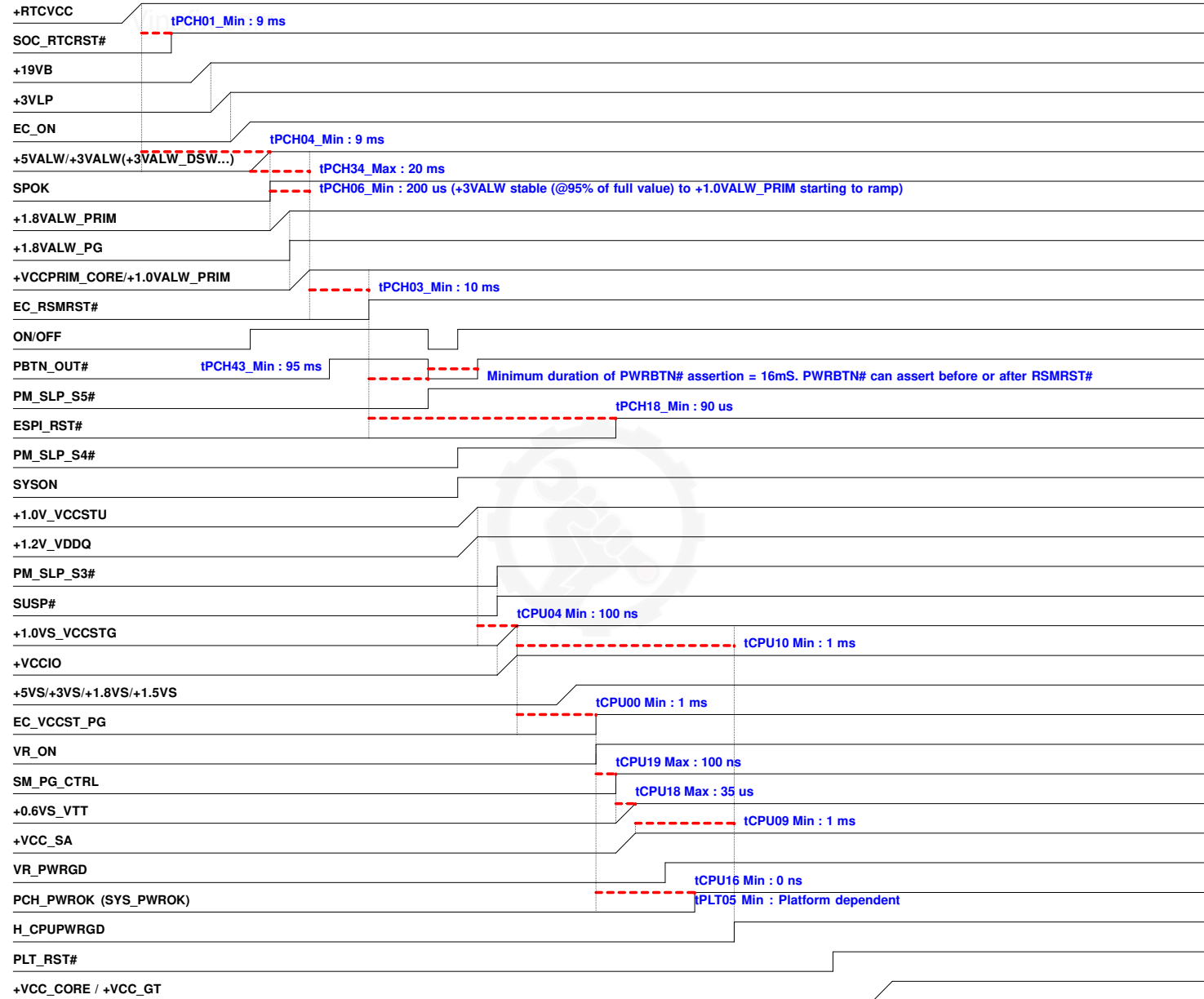
Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on



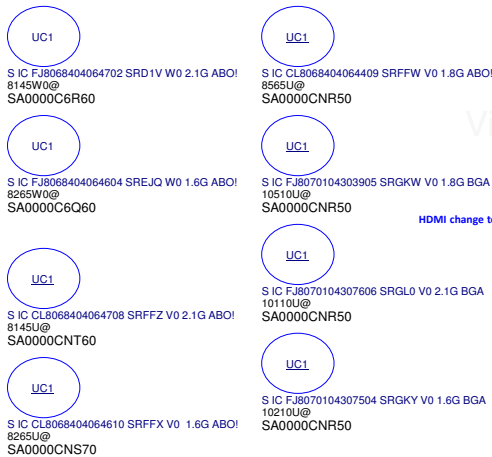
I2C Address Table

BUS	Device	Address (8 bit)
I2C_0 (+3VS)	Reserved	
I2C_1 (+3VALW_PRIM)	TM-P3393-003 (TP)	0x2C
	FA577E-1206 (TP-ELAN)	0x15
	SA577C-12A0 (TP-ELAN)	0x15
SOC_SMBCLK (+3VS)	SO-DIMM2	0xA4
	G-Sensor	0x30
SOC_SML1CLK (+3VALW_PRIM)	EC	
EC_SMB_CK1 (+3VLP)	BQ24781 (Charger IC)	0x12
	BATTERY PACK	0x16

PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



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HDMI change to DD12 port 11/26

HDMI

HDMI DDC (Port B)

<22> SOC_DP2_CTRL_CLK
<22> SOC_DP2_CTRL_DATA

EDP_COMP

AM6

DISP_RCOMP

CG8

CG9

CH4

CH3

CP4

CN4

CR26

CP26

WHL-U42_BGA1528

@

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DDI

DDI1_TXN_0

DDI1_TXN_1

DDI1_TXP_1

DDI1_TXN_2

DDI1_TXP_2

DDI1_TXN_3

DDI1_TXP_3

DDI2_TXN_0

DDI2_TXP_0

DDI2_TXN_1

DDI2_TXP_1

DDI2_TXN_2

DDI2_TXP_2

DDI2_TXN_3

DDI2_TXP_3

DDI3_TXN_0

DDI3_TXP_0

DDI3_TXN_1

DDI3_TXP_1

DDI3_TXN_2

DDI3_TXP_2

DDI3_TXN_3

DDI3_TXP_3

DDI3_TXN_4

DDI3_TXP_4

DDI3_TXN_5

DDI3_TXP_5

DDI3_TXN_6

DDI3_TXP_6

DDI3_TXN_7

DDI3_TXP_7

DDI3_TXN_8

DDI3_TXP_8

DDI3_TXN_9

DDI3_TXP_9

DDI3_TXN_10

DDI3_TXP_10

DDI3_TXN_11

DDI3_TXP_11

DDI3_TXN_12

DDI3_TXP_12

DDI3_TXN_13

DDI3_TXP_13

DDI3_TXN_14

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DDI3_TXN_15

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DDI3_TXN_87

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DDI3_TXN_100

DDI3_TXP_100

DDI3_TXN_101

DDI3_TXP_101

DDI3_TXN_102

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DDI3_TXN_103

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DDI3_TXN_110

DDI3_TXP_110

DDI3_TXN_111

DDI3_TXP_111

DDI3_TXN_112

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DDI3_TXN_114

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DDI3_TXN_118

DDI3_TXP_118

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DDI3_TXP_119

DDI3_TXN_120

DDI3_TXP_120

DDI3_TXN_121

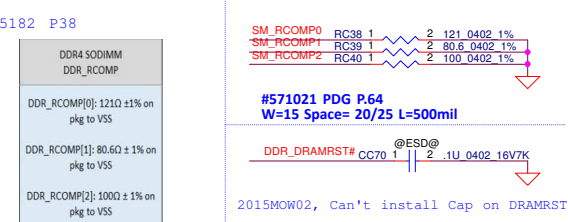
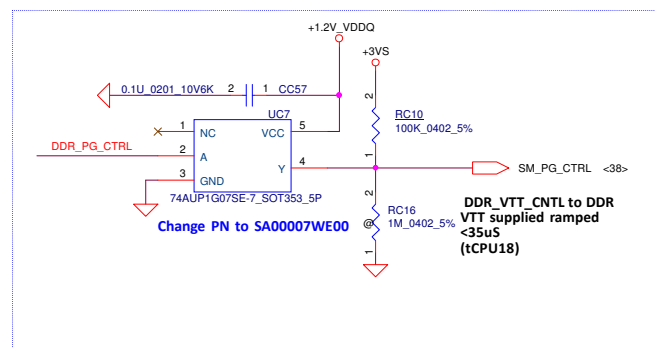
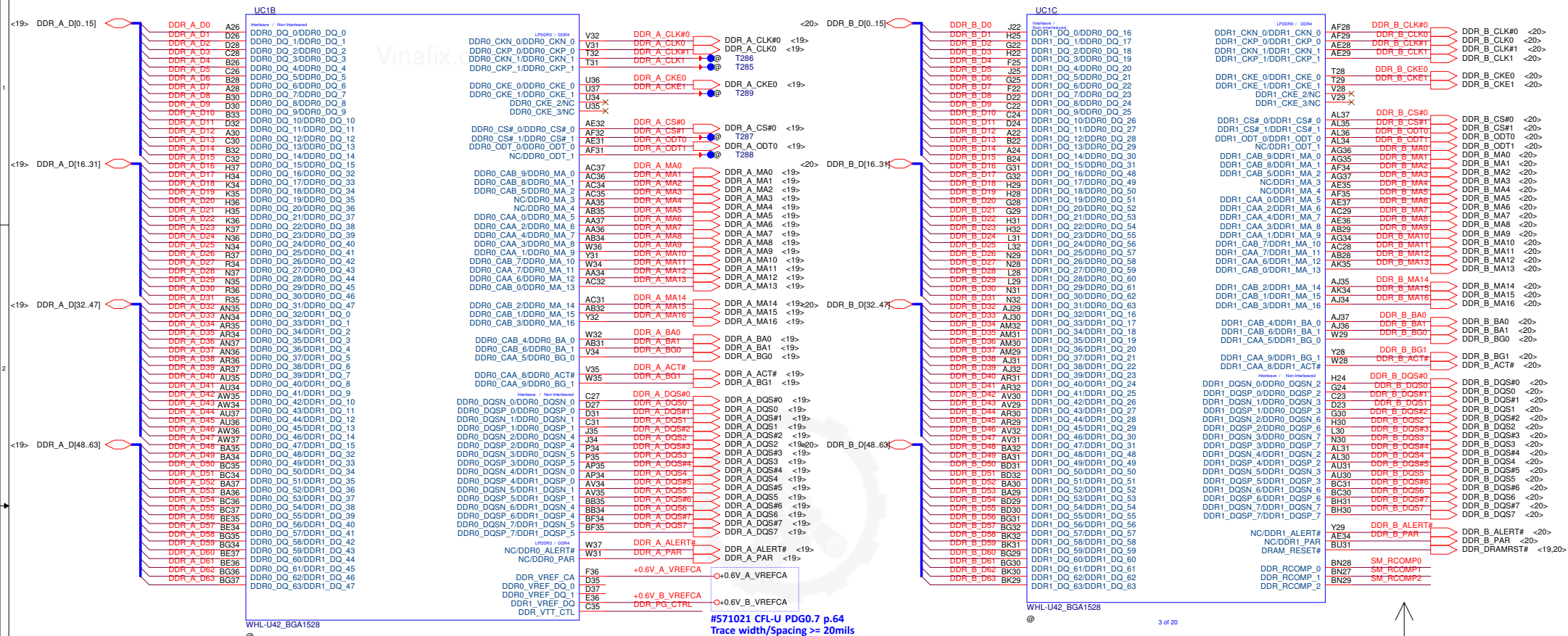
DDI3_TXP_121

DDI3_TXN_122

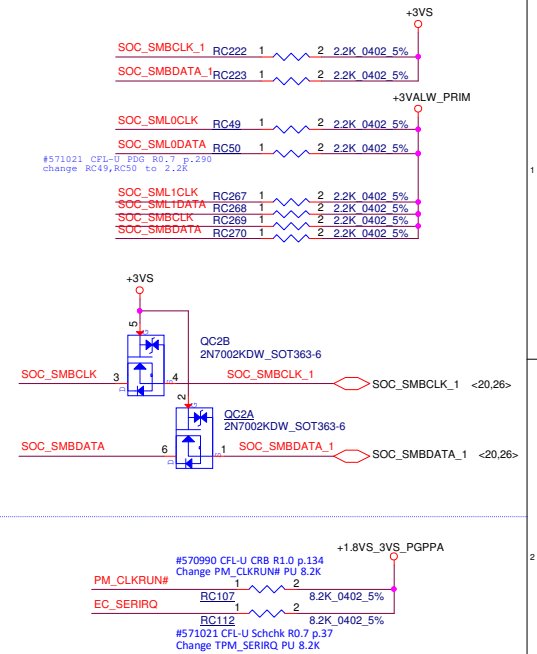
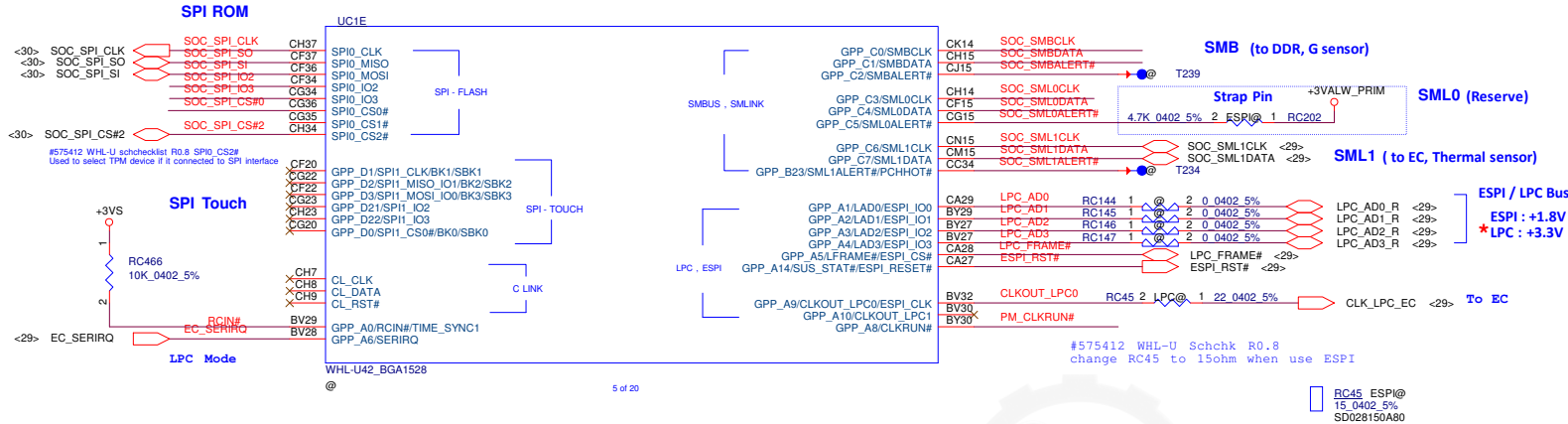
DDI3_TXP_122

DDI

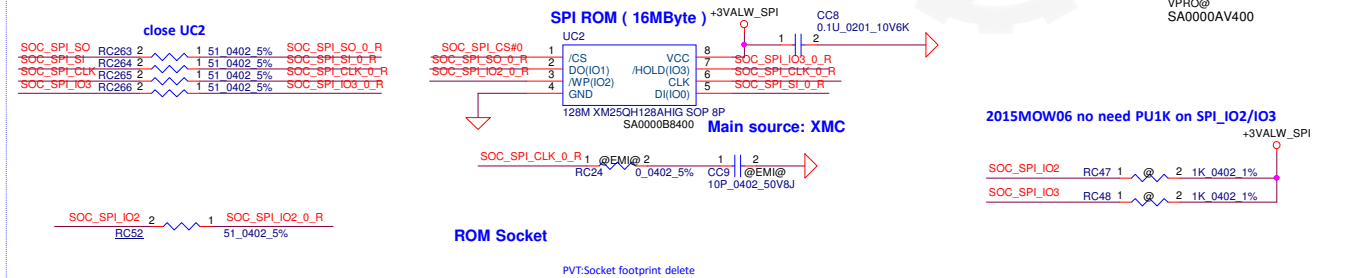
Interleaved Memory



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#575412 WHL-U schck R0.
 50Q series resistor: 3.3V
 33Q series resistor: 1.8V



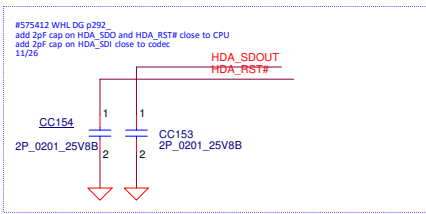
SML0ALERT# / GPP_C5 (Internal Pull Down):
 (Sampled: Rising edge of RSMRST#)

eSPI or LPC
 * 0 = LPC is selected for EC --> For KB9022/9032 Use
 1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
 (Sampled: Rising edge of RSMRST#)

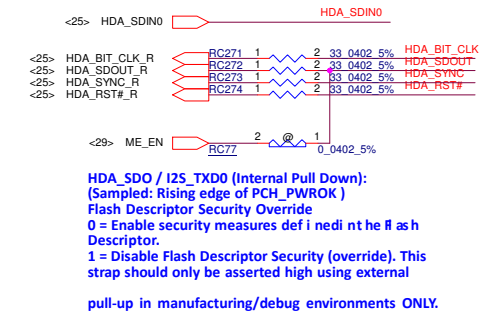
TLS Confidentiality
 * 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
 1 = Enable Intel ME Crypto (TLS) (with confidentiality).
 Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

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Deciphered Date				2019/12/27				WHL-U(3/12)SPI,ESPI,SMB,LPC			
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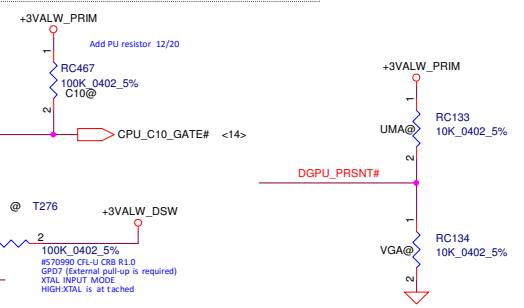
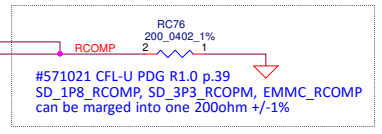
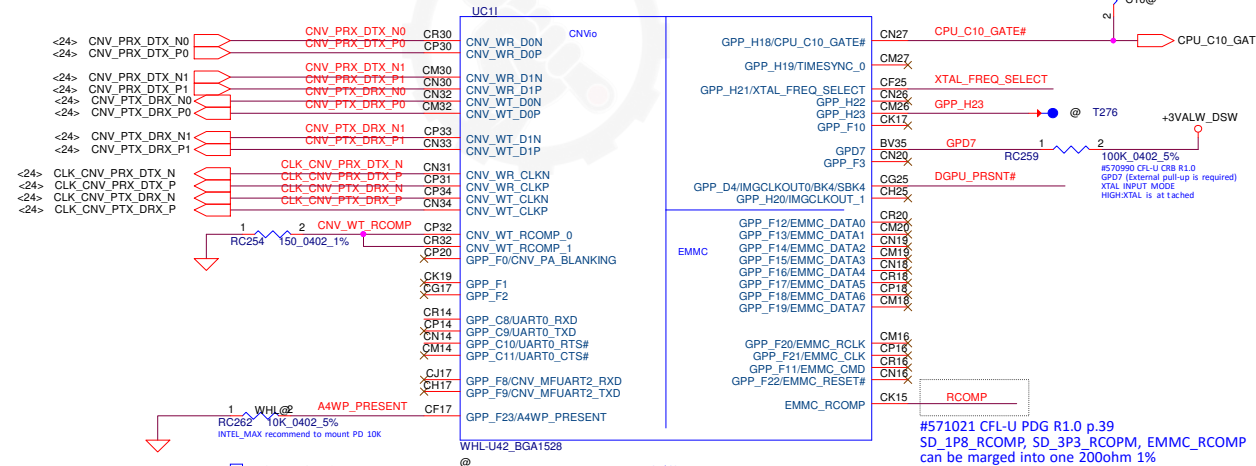
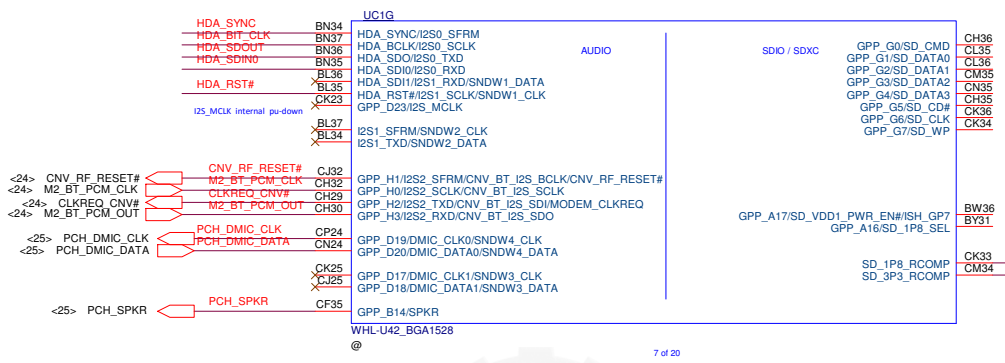
HDA for AUDIO



SPKR / GPP_B14 (Internal Pull Down): (Sampled: Rising edge of PCH_PWROK)

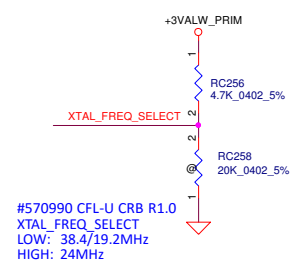
- * **TOP Swap Override**
0 = Disable TOP Swap mode.
1 = Enable TOP Swap Mode.

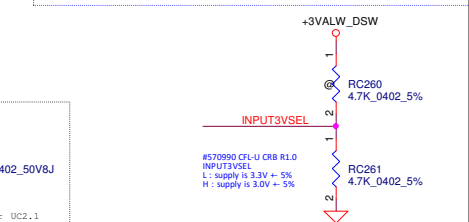
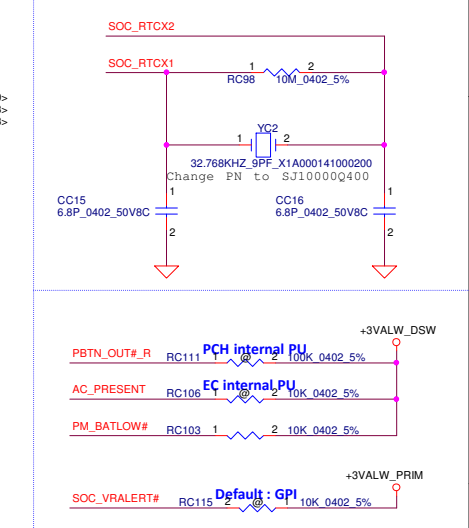
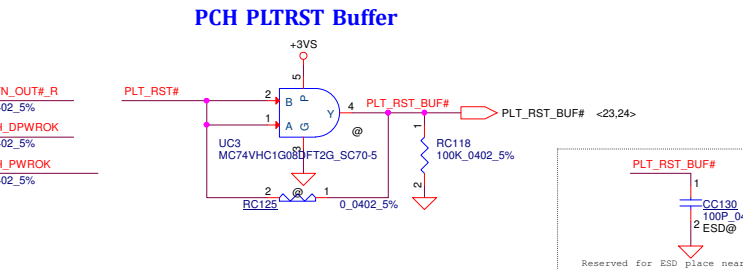
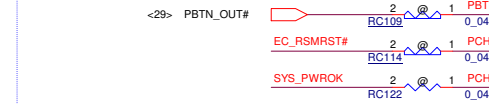
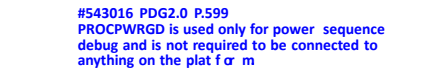
Intel HD Audio link capabilities
> Two SDI signals to support two external codecs.
> Drivers variable frequency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
> SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



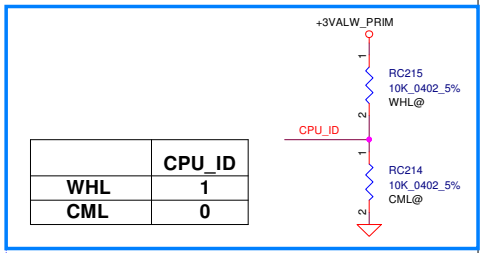
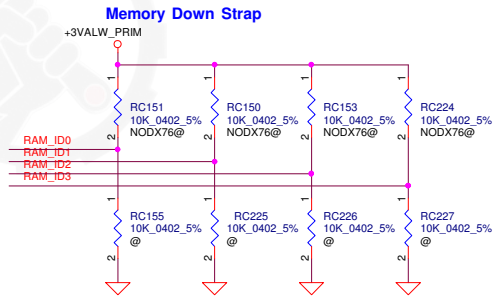
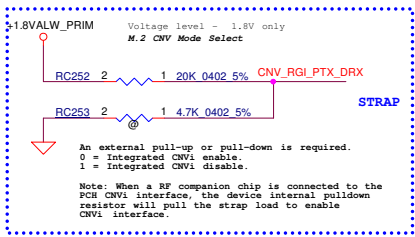
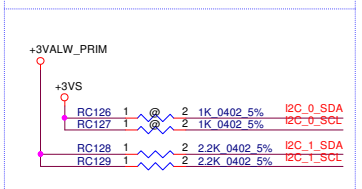
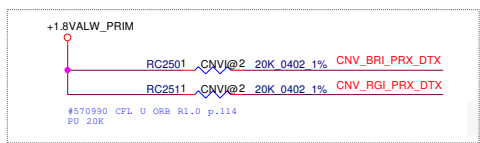
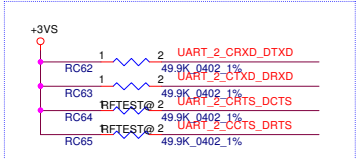
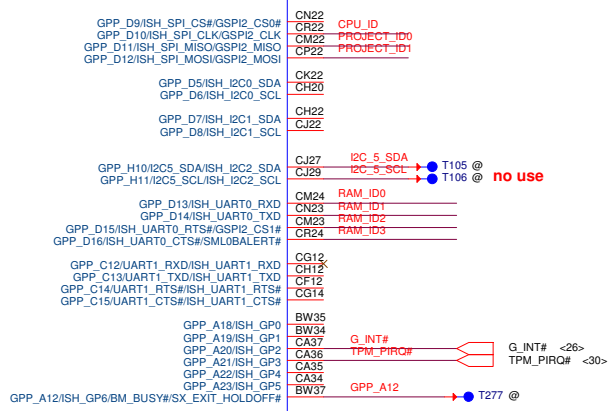
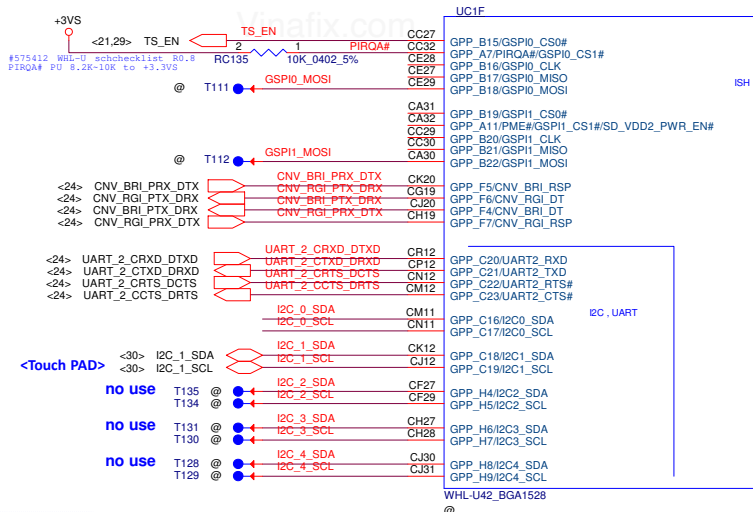
	DGPU_PRSN#
DIS, Optimus	0
UMA	1

#571021 CFL-U PDG R1.0 p.39
SD_1P8_RCOMP, SD_3P3_RCOMP, EMMC_RCOMP
can be merged into one 200ohm 1%

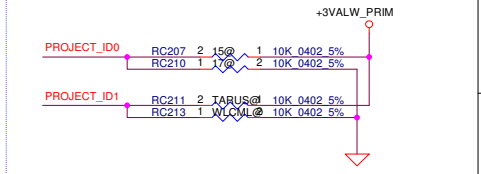




Security Classification		Compal Secret Data		Compal Electronics, Inc. WHL-U(S12)CLK,GPIO	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
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				Custom	EH7LW M/B LA-H792P
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				Sheet	11 of 46
				Rev	0.1



WHL	CPU_ID
1	0



Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* EH7LW/FH7LC	0	0
EH5LW/FH5LC	0	1
NA	1	0
FH5TW	1	1

Functional Strap Definitions

GSPi0_MOSI / GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPi1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*0 = SPI Mode --> AAX05 Use
1 = LPC Mode

- ZZZ1 Hynix4GB X76DHYN@ X76829BOL04
- ZZZ2 Micron4GB X76DMIC@ X76829BOL05
- ZZZ3 Samsung4GB X76DSAM@ X76829BOL06

	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000BMN30 (S IC D4 512M16 H5AN8G6NCUR-VKC FBGA ABOI)
Micron 4GB	0	0	0	1	SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABOI)
Samsung 4GB	0	0	1	0	SA0000B6F00 (S IC D4 512M16 K4A8G165WC-BCTD FBGA 96P)
No OnBoard Memory	1	1	1	1	No On Board Memory

11/28
For layout routing
PCIE P5/P6 exchange

NGFF WLAN+BT (Key E)

GLAN

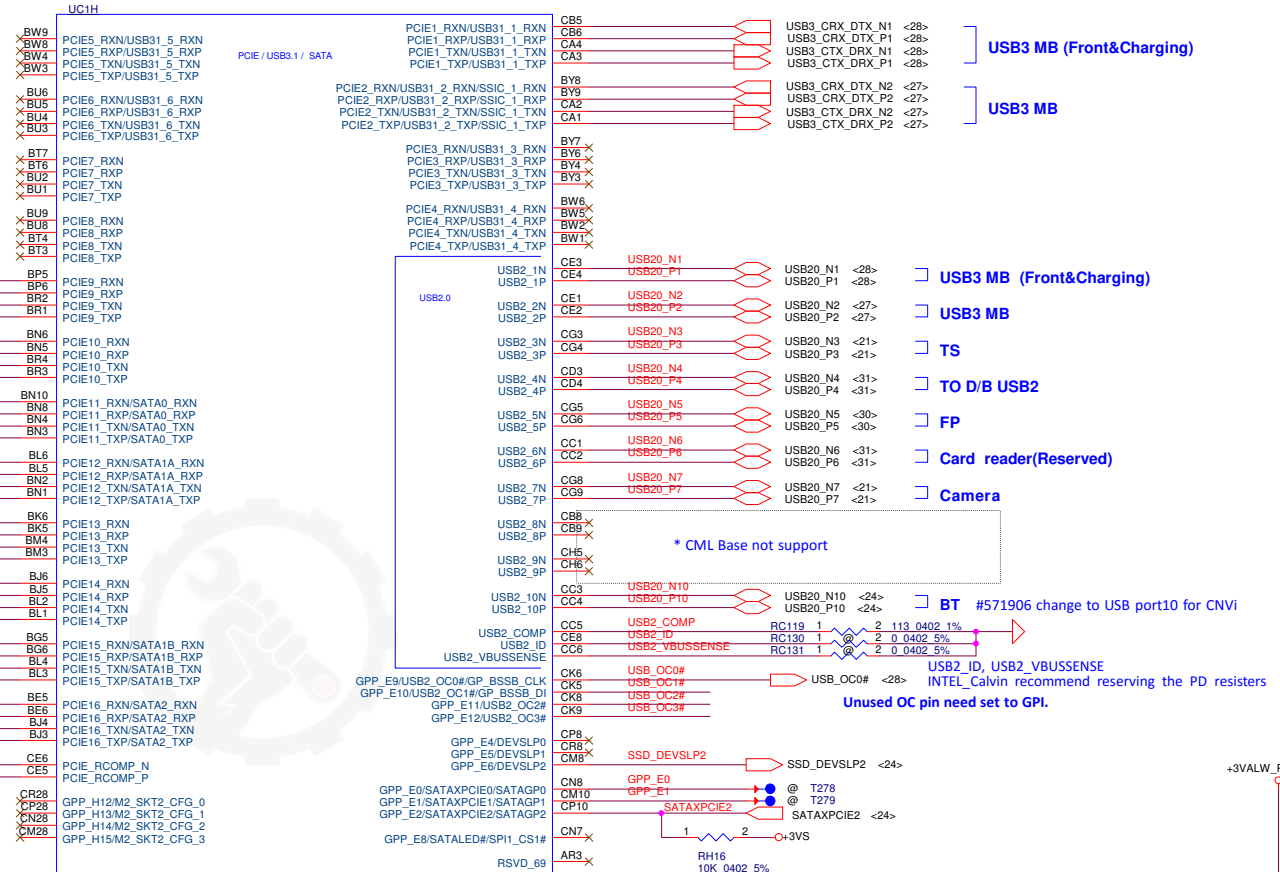
HDD

ODD

NGFF SSD (Key M)
(Need Lane Reversal)

* CML Base not support SATA func i on

#575412 p.46
PCIE_RCOMP_N/PCIE_RCOMP_P
R=100ohm



6.1.2.1 Cannon Lake U (CNL U) PCH-LP

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIE* #7	PCIE* #8	PCIE* #9	PCIE* #10	PCIE* #11	PCIE* #12	PCIE* #13	PCIE* #14	PCIE* #15	PCIE* #16
	PCIE* #1	PCIE* #2	PCIE* #3	PCIE* #4	PCIE* #5	PCIE* #6	GHE	GHE	GHE	SATA 0	SATA 1a	GHE	GHE	SATA 1b	SATA 2	SATA 2
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

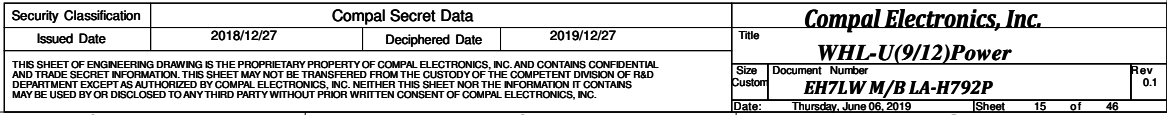
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.

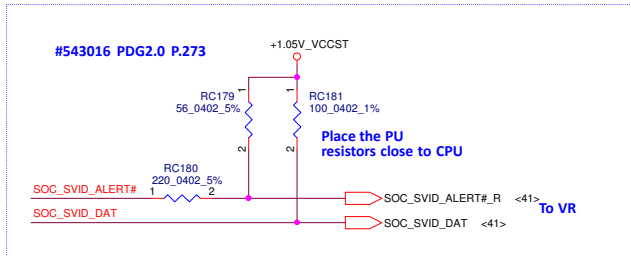
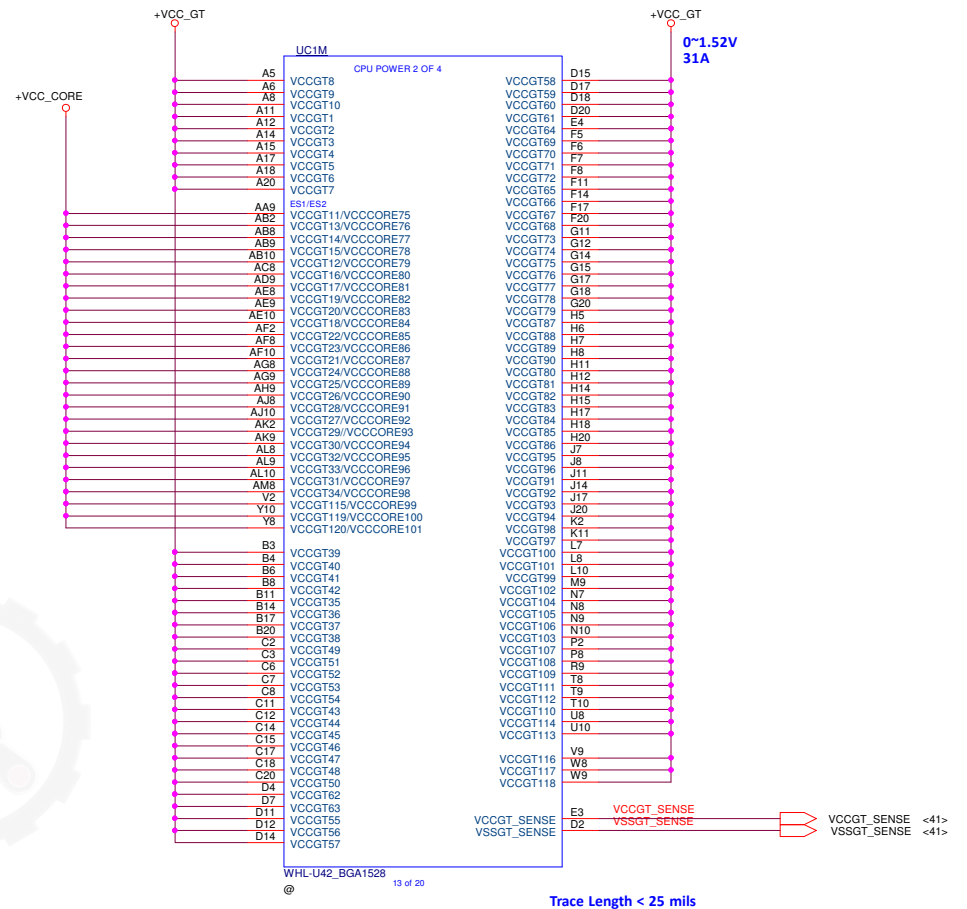
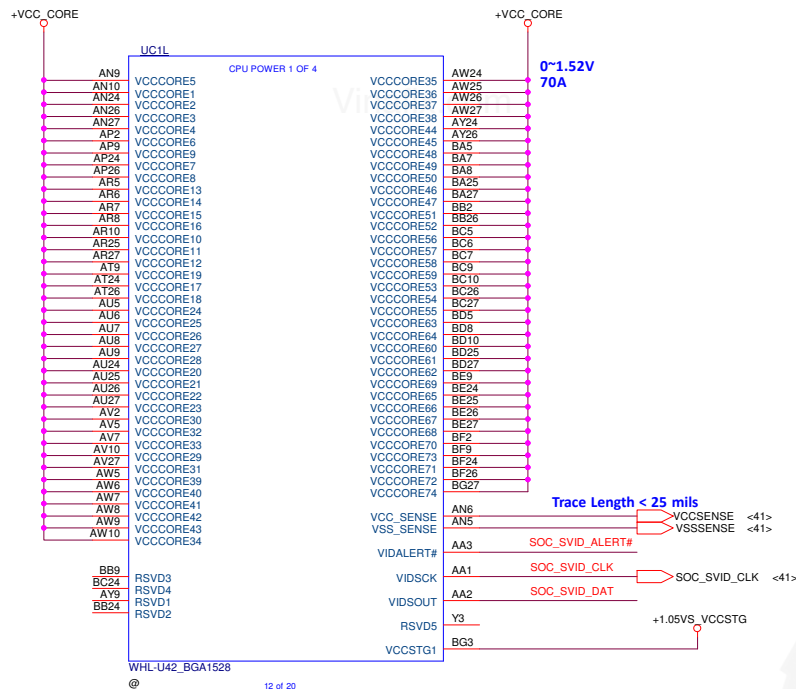
- When high DEVSLP requests the SATA device to enter into the DEVSLP power state
- When low DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
- When used as an interlock switch status indicator, this signal should be driven to 0 to indicate that the switch is closed and to 1 to indicate that the switch is open.
- If mechanical presence switches will not be used on the platform SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

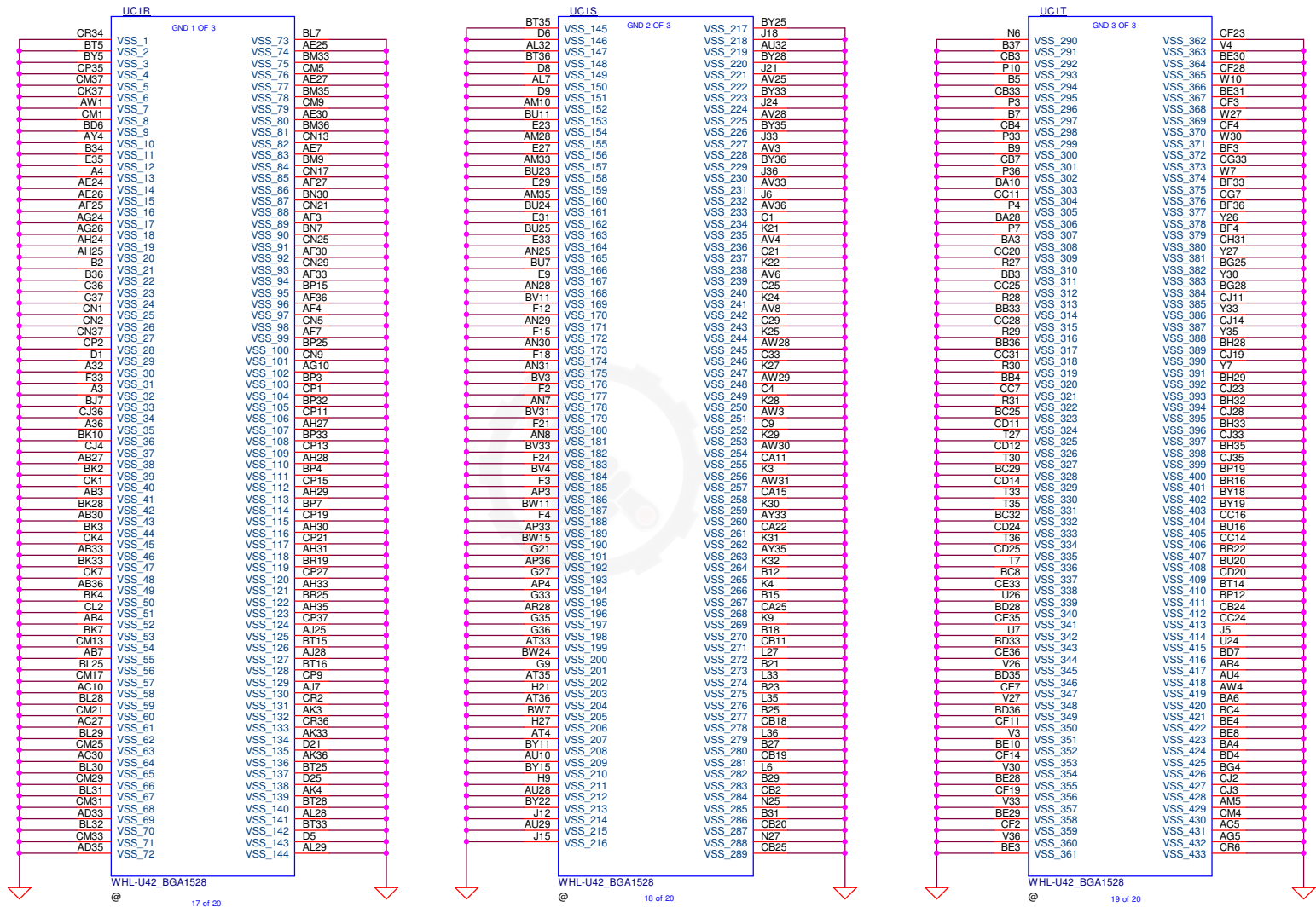
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Issued Date	2018/12/27	Deciphered Date	2019/12/27	Customer
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Compal Electronics, Inc.				Document Number
WHL-U(7/12)PCIE,USB,SATA				EH7LW M/B LA-H792P
Date: Thursday, June 06, 2019				Sheet 13 of 46



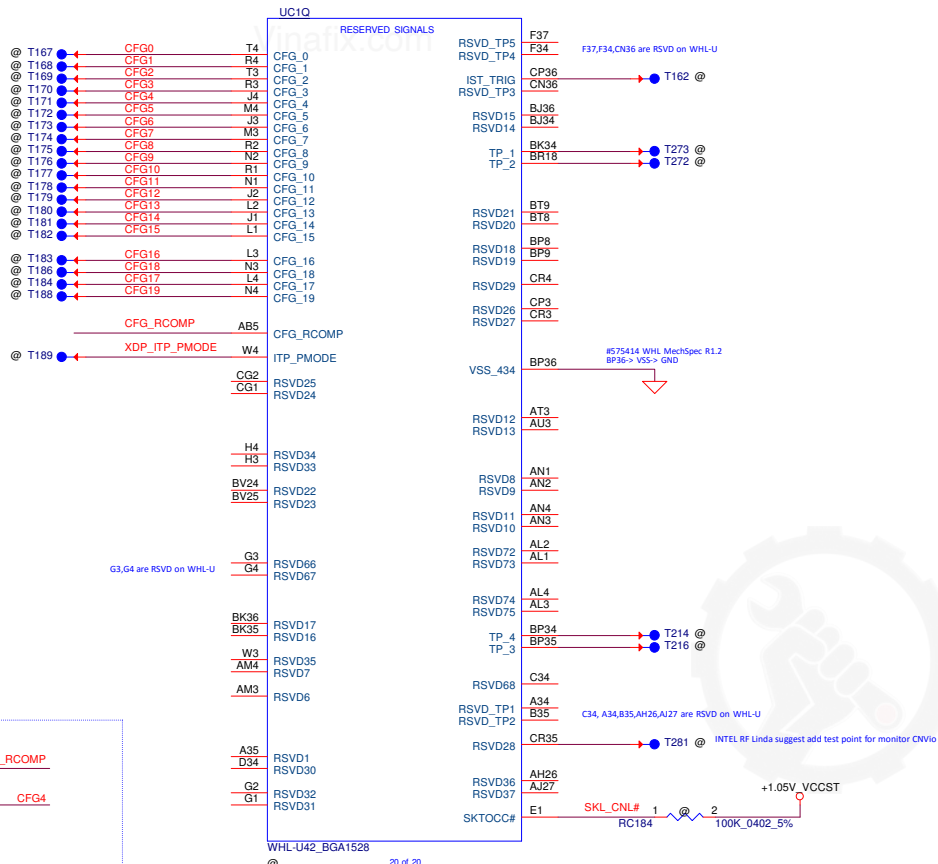


Processor Power Rails

Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

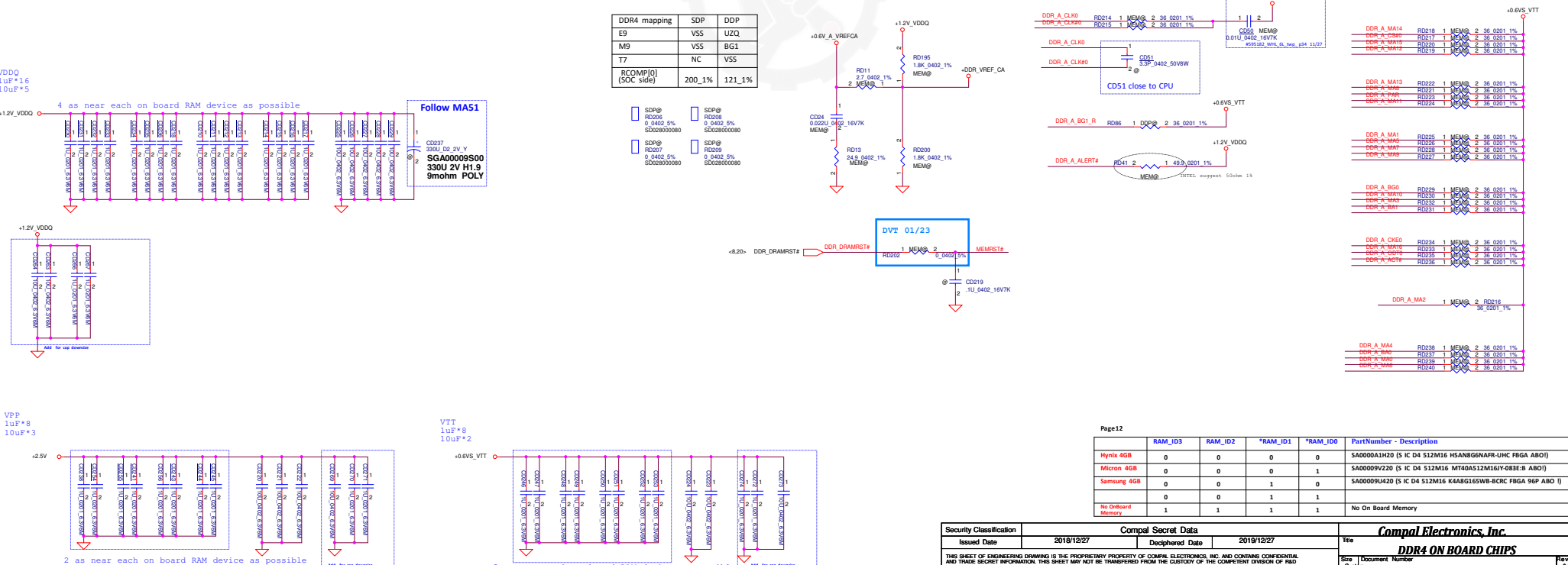
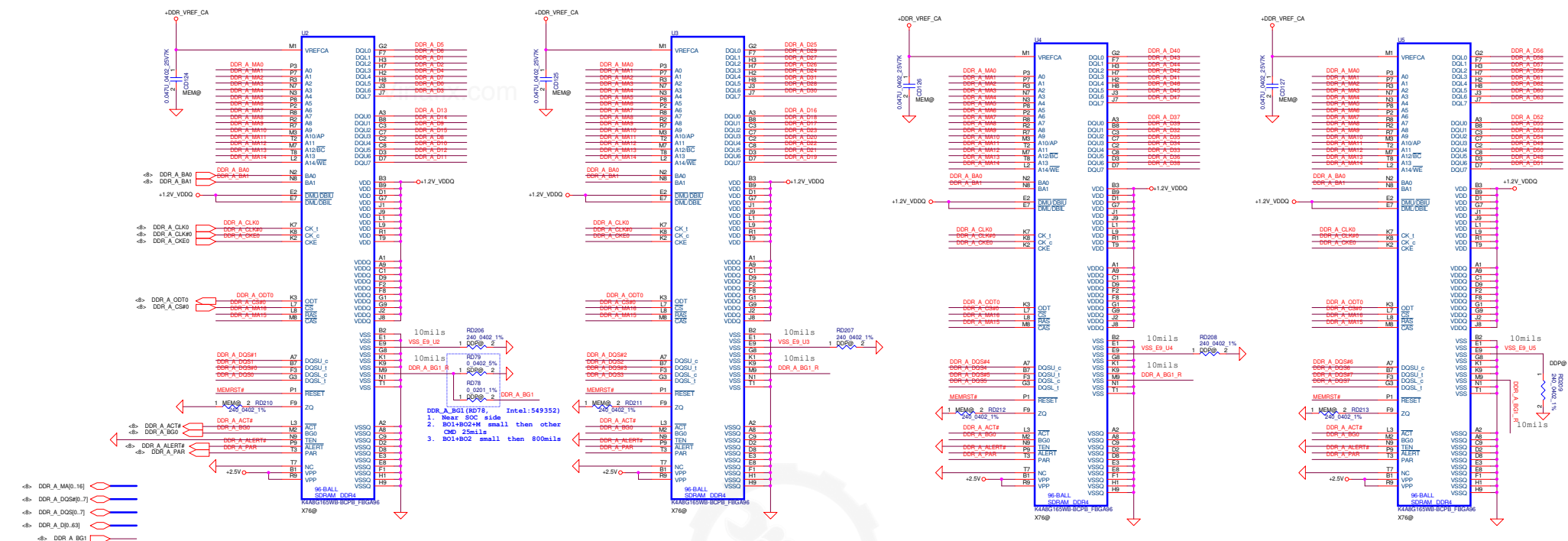


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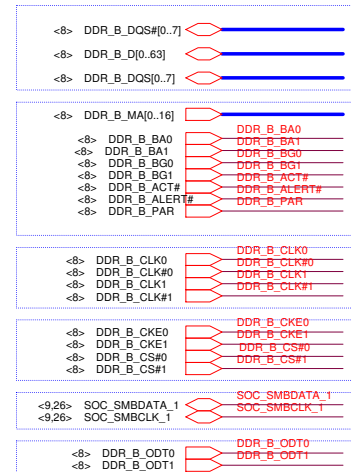
#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port at tached to E mbedded Dsplay Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

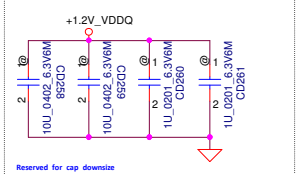
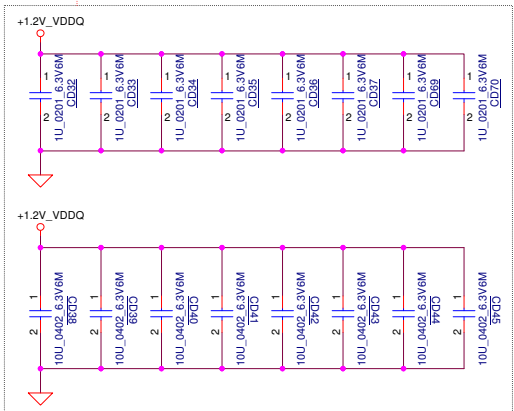


TERMINATION

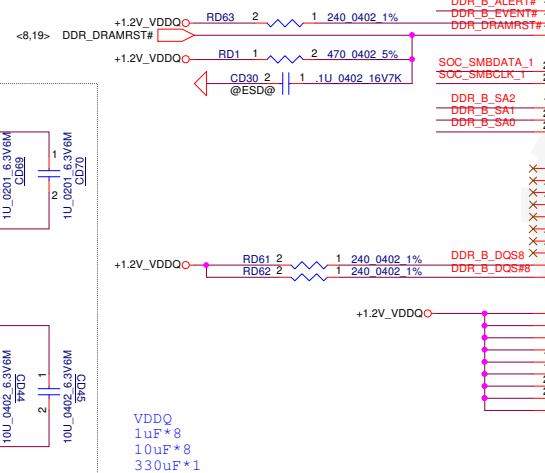
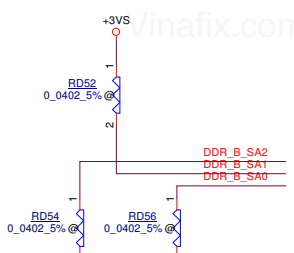
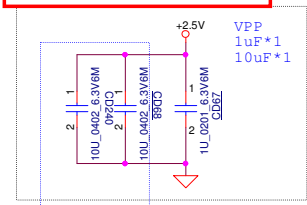
Page12	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
	Hylix 4GB	0	0	0	SA000A1H20 (S IC D4 512M16 HSAN8G6N4NR-UHC FBGA ABOI)
	Microon 4GB	0	0	1	SA0009V220 (S IC D4 512M16 MT40A512M16Y-08SE-B ABOI)
	Samsumg 4GB	0	0	1	SA0009U420 (S IC D4 512M16 KA48G16SWB-BCHC FBGA 96P ABO I)
		0	0	1	
		1	1	1	No On Board Memory



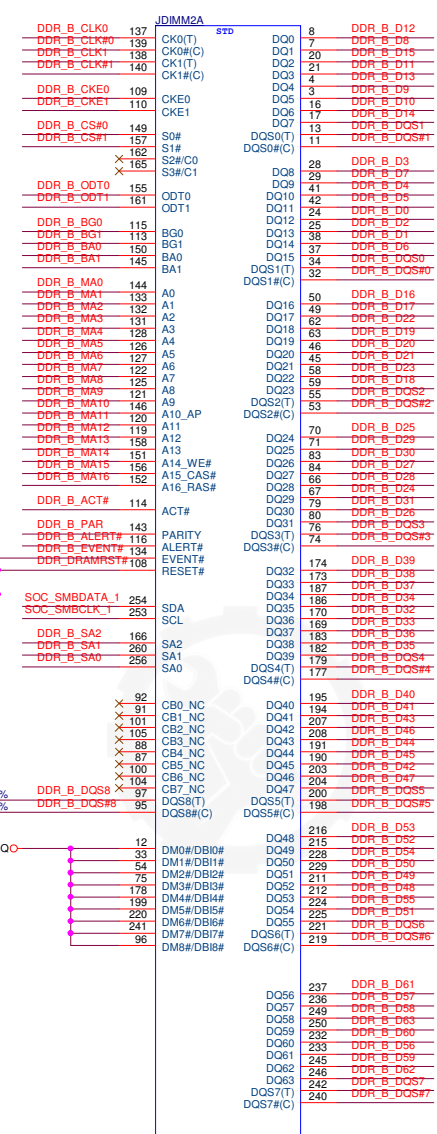
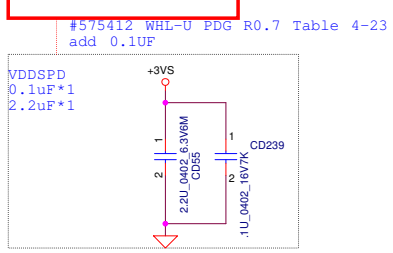
Layout Note:
Place near JDIMM2



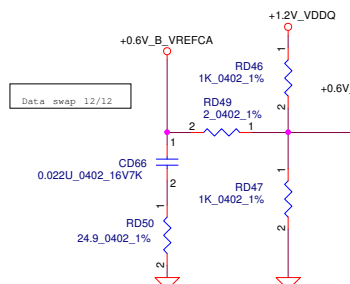
Layout Note:
Place near JDIMM1.257,259



Layout Note:
Place near JDIMM2.255

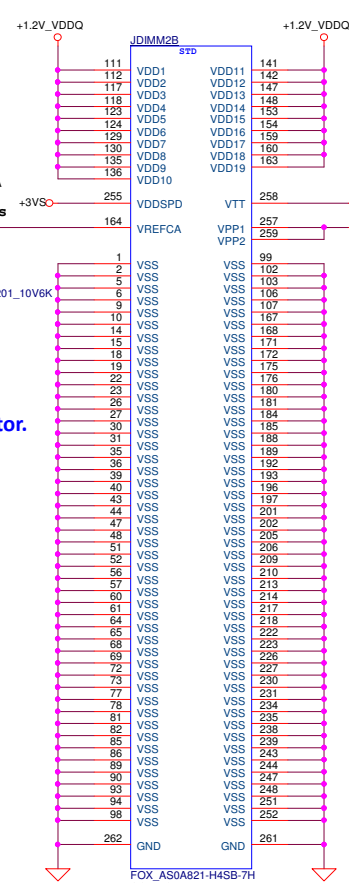


Compatible with SP07001HW00

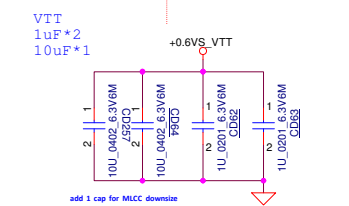


Place near to SO-DIMM connector.

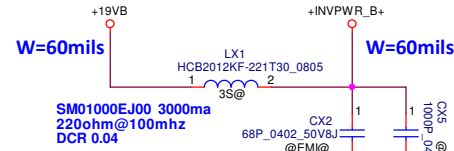
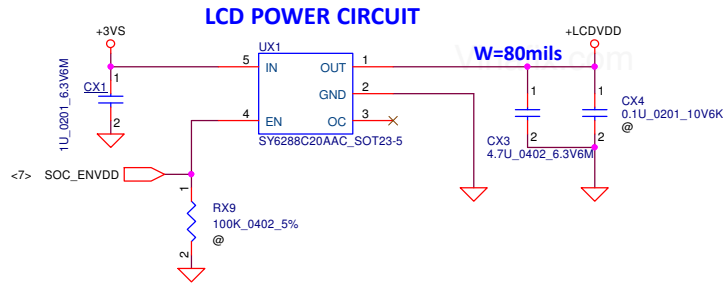
Standard Type
2-3A to 1 DIMMs/channel



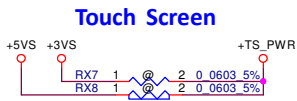
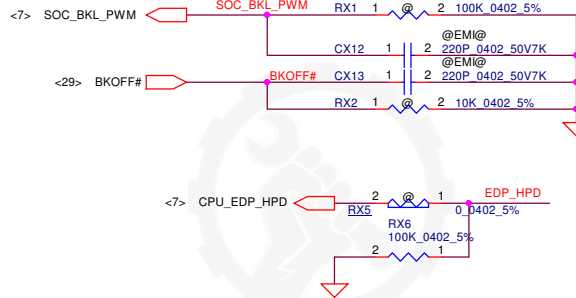
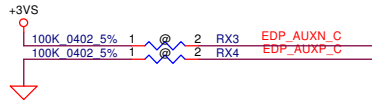
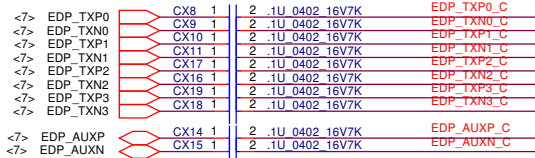
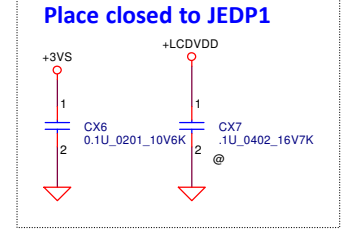
Layout Note:
Place near JDIMM1.258



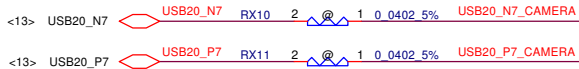
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2018/12/27				DDR4 DIMMB			
Deciphered Date				2019/12/27				EH7LW M/B LA-H792P			
Title				20				Rev 0.1			
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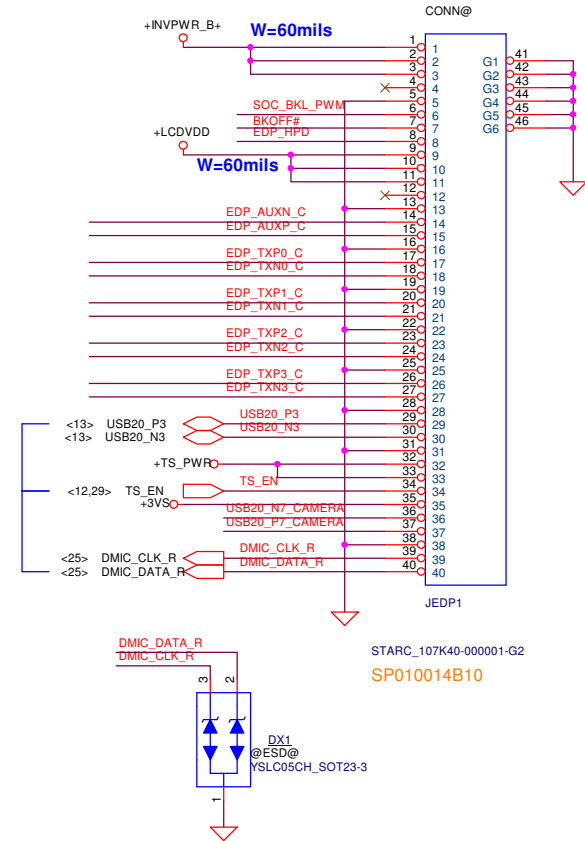
Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)



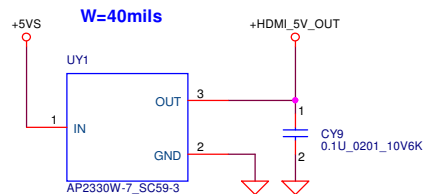
Camera



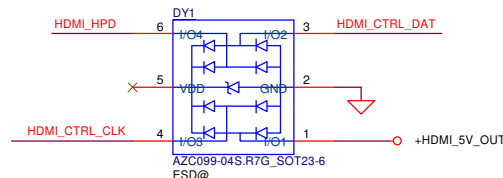
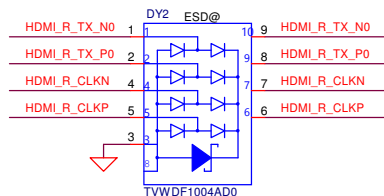
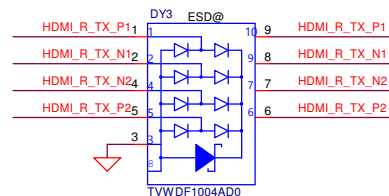
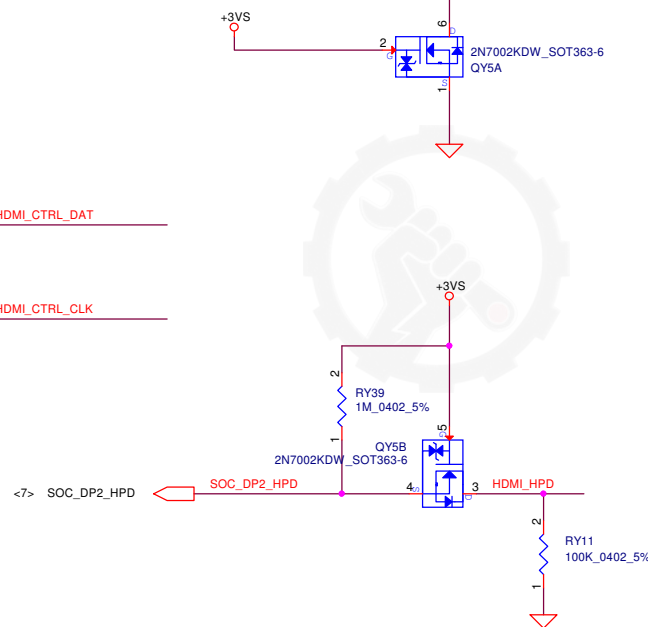
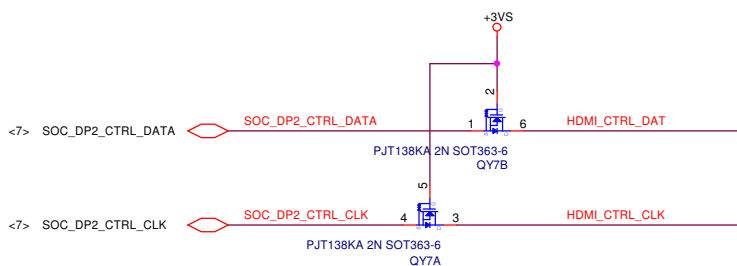
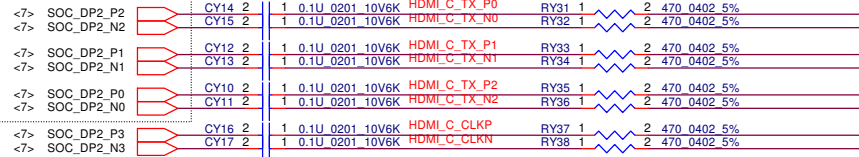
Touch Screen
For Camera



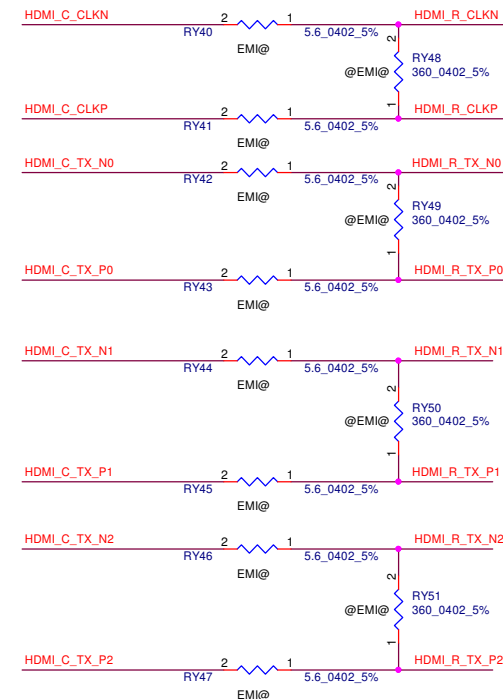
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2018/12/27		Deciphered Date		2019/12/27		Title			
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						Size		Document Number		Rev	
						Custom		EH7LW M/B LA-H792P		0.1	
Date:		Thursday, June 06, 2019		Sheet		21		of 46			



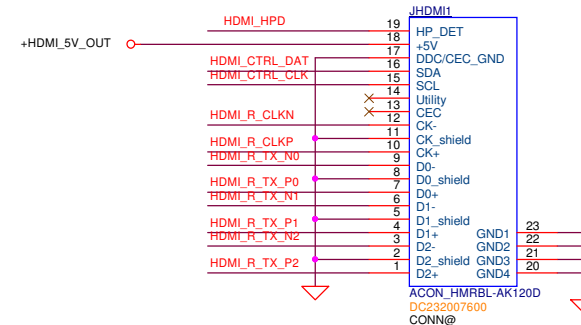
port 0, 2 swap for INTEL HDMI



P/N: SC300001G00,S DIO(BR) AZC099-04S.R7G SOT23 ESD



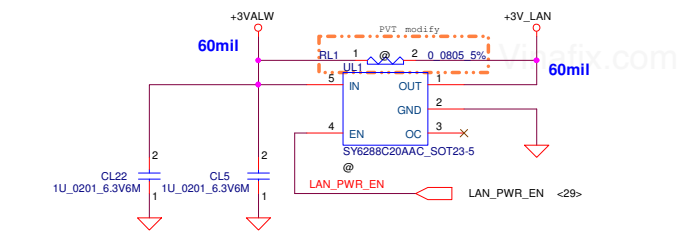
HDMI connector



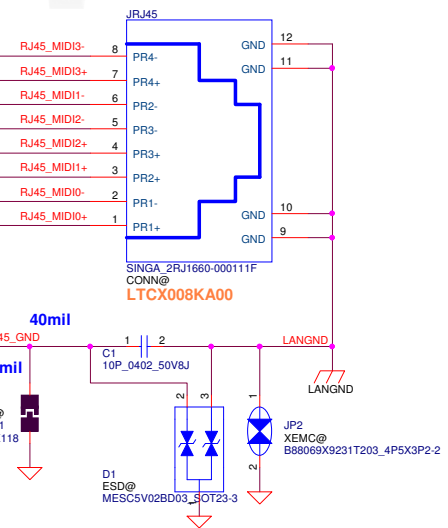
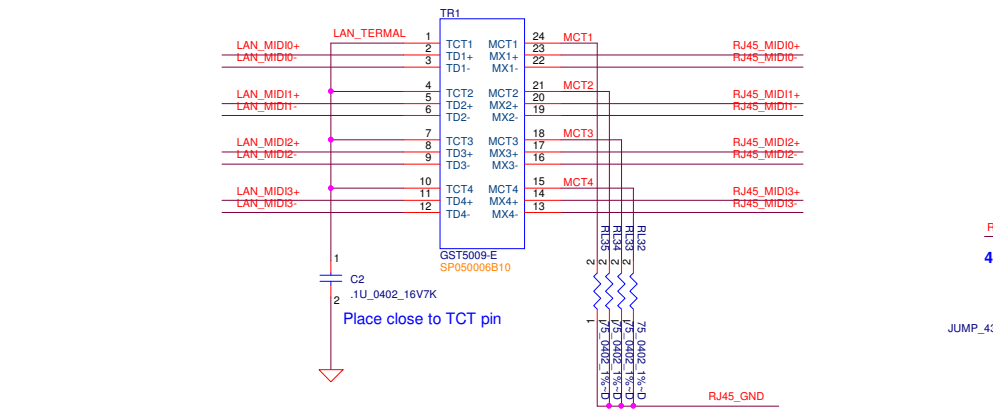
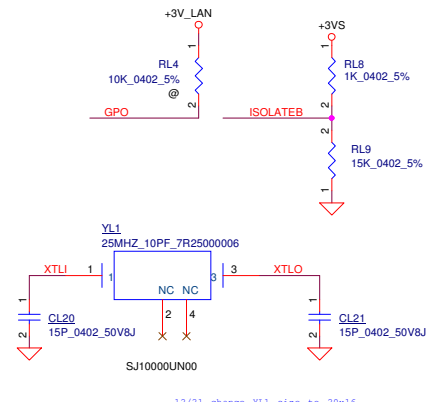
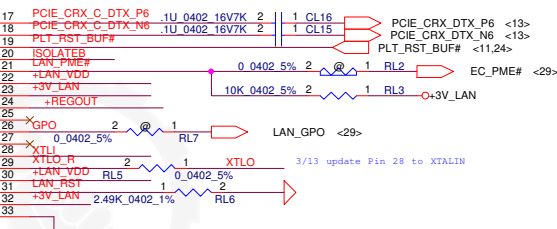
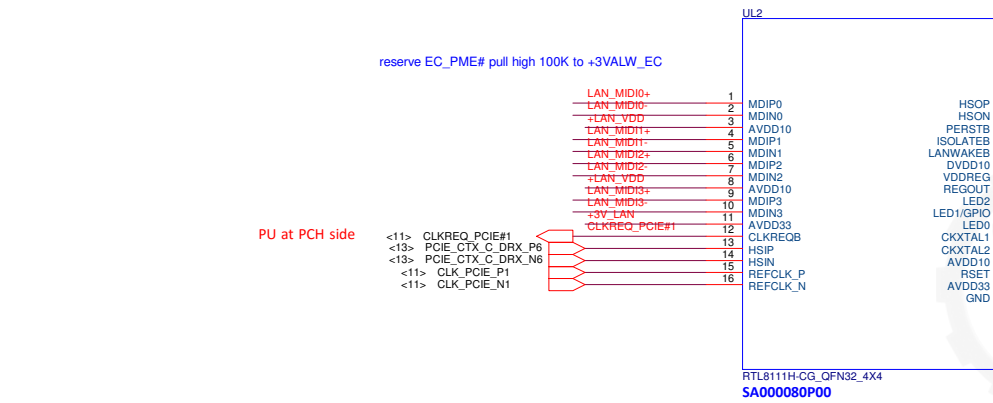
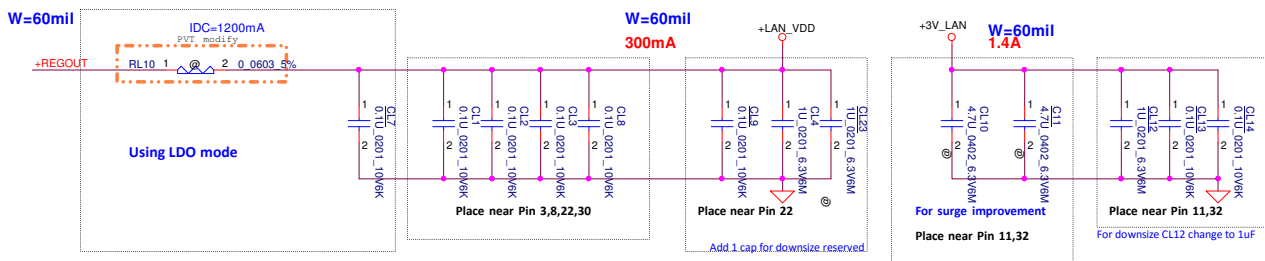
SYMBOL: DC232004700

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				Size	Document Number			Rev
				Custom	EH7LW M/B LA-H792P			
				Date:	Thursday, June 06, 2019		Sheet	22

LAN-RTL8111H



From EC
High active
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms

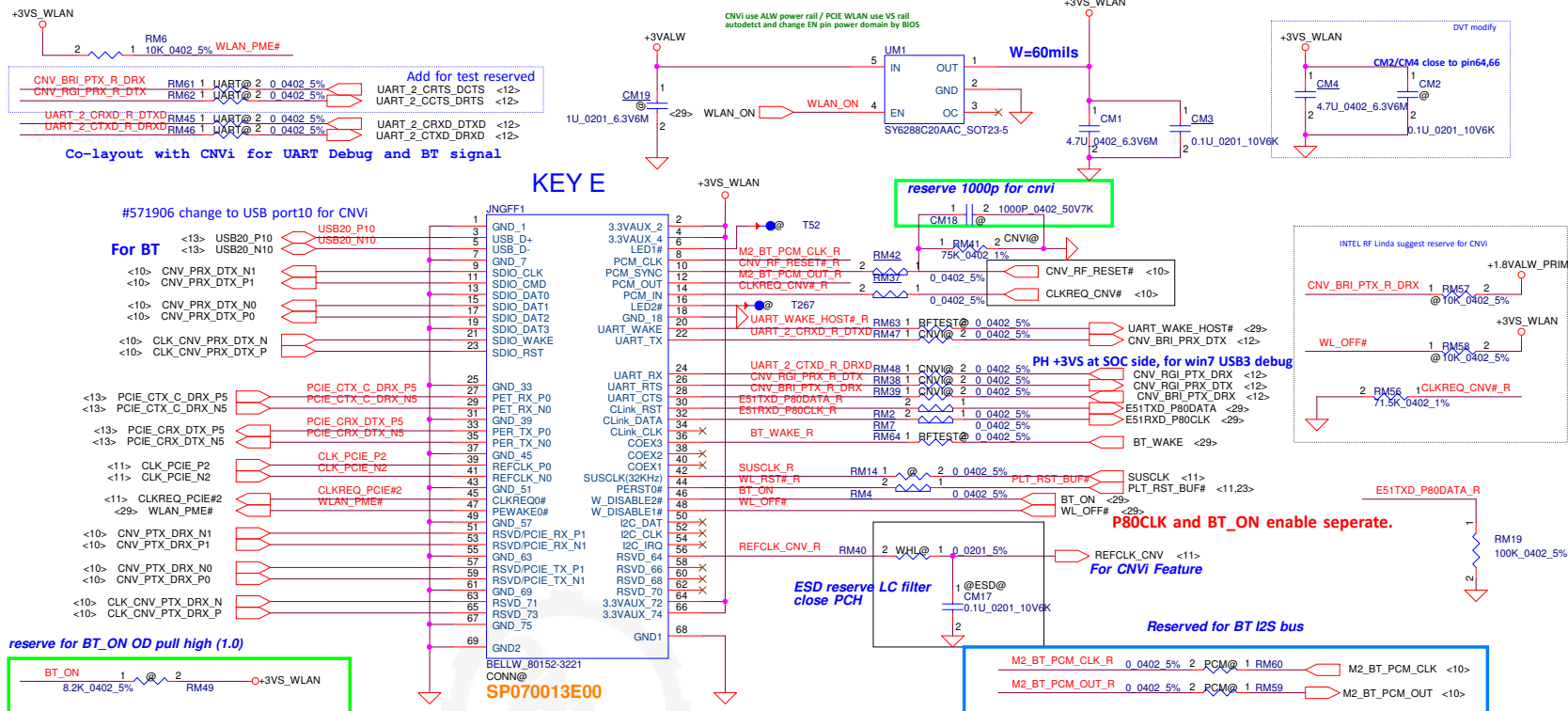


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		Deciphered Date		LAN RTL8111H-CG	
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				Document Number	
				EH7LW M/B LA-H792P	
				Date: Friday, August 02, 2019	
				Sheet 23 of 46	
				Rev 0.1	

Wireless LAN

NGFF WL+BT (KEY E)

74	3.0V	GND	75
70	3.0V	RESERVED/PE/CAN1	76
72	UM_Power_SMC/IO/PWakeUp	RESERVED/PE/CPU2	77
68	UM_Power_SMC/CLKREQ	GND	69
66	UM_SVP/PERST1	Reserved/PE/Ext	67
64	RESERVED	Reserved/PE/DQ1	65
62	ALERT1	GND	63
60	QDCC (IO0/0.3)	Reserved/PE/T1	61
58	QDCTA (IO0/0.3)	Reserved/PE/D1	59
56	W_DISABLE1 (IO0/0.3V)	GND	57
54	Reserved/W_DISABLE1 (IO0/0.3V)	RESERVED/IO0/0.3V	55
52	PERST0 (IO0/0.3)	CLKREQ0 (IO0/0.3V)	53
50	SUIC1 (IO0/0.3V)	GND	51
48	COOL1 (IO0/0.1.8V)	REFCLK0	49
46	COOL2 (IO0/1.8V)	REFCLK0	47
44	COOL0 (IO0/1.8V)	PERNO	45
42	VENDOR DEFINED	PERNO	43
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERIO	37
36	UART15 (IO0/1.8V)	PERIO	35
34	UART15 (IO0/1.8V)	GND	33
32	UART15 (IO0/1.8V)	GND	31
22	UART16 (IO0/1.8V)	SIO_RESET (IO0/1.8V)	23
20	UART Wakeup (IO0/1.8V)	SIO_Wakeup (IO0/1.8V)	21
18	GND	SIO_DAT17 (IO0/1.8V)	19
16	LED11 (I/O)	SIO_DAT16 (IO0/1.8V)	17
14	POL_OUT105_SQ_OUT (IO0/1.8V)	SIO_DAT15 (IO0/1.8V)	15
12	POL_IN432_SQ_IN (IO0/1.8V)	SIO_DAT14 (IO0/1.8V)	13
10	POL_SYNC123_HS (IO0/1.8V)	SIO_CLK10 (IO0/1.8V)	11
8	POL_CLK12368 (IO0/1.8V)	SIO_CLK10 (IO0/1.8V)	9
6	LED11 (I/O)	GND	7
4	3.0V	USB_D-	5
2	3.0V	USB_D+	3
		GND	

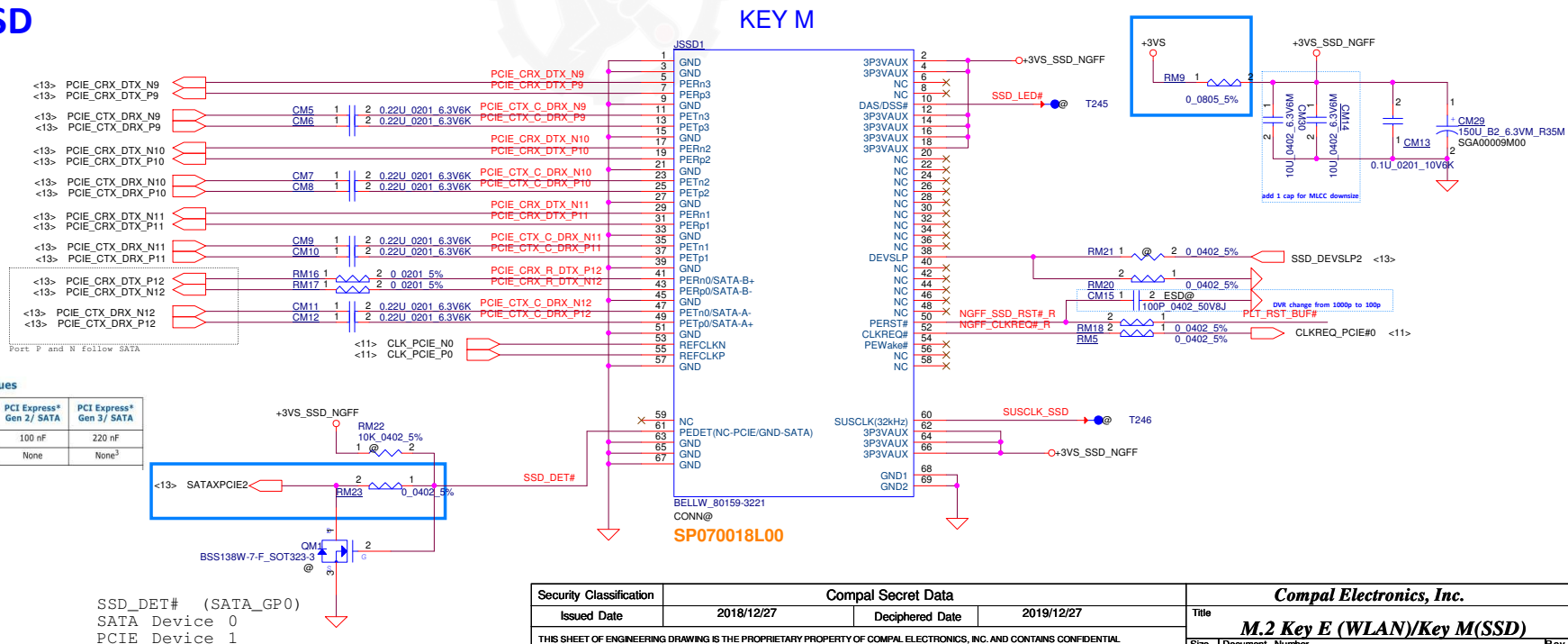


mSATA/SSD

PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41

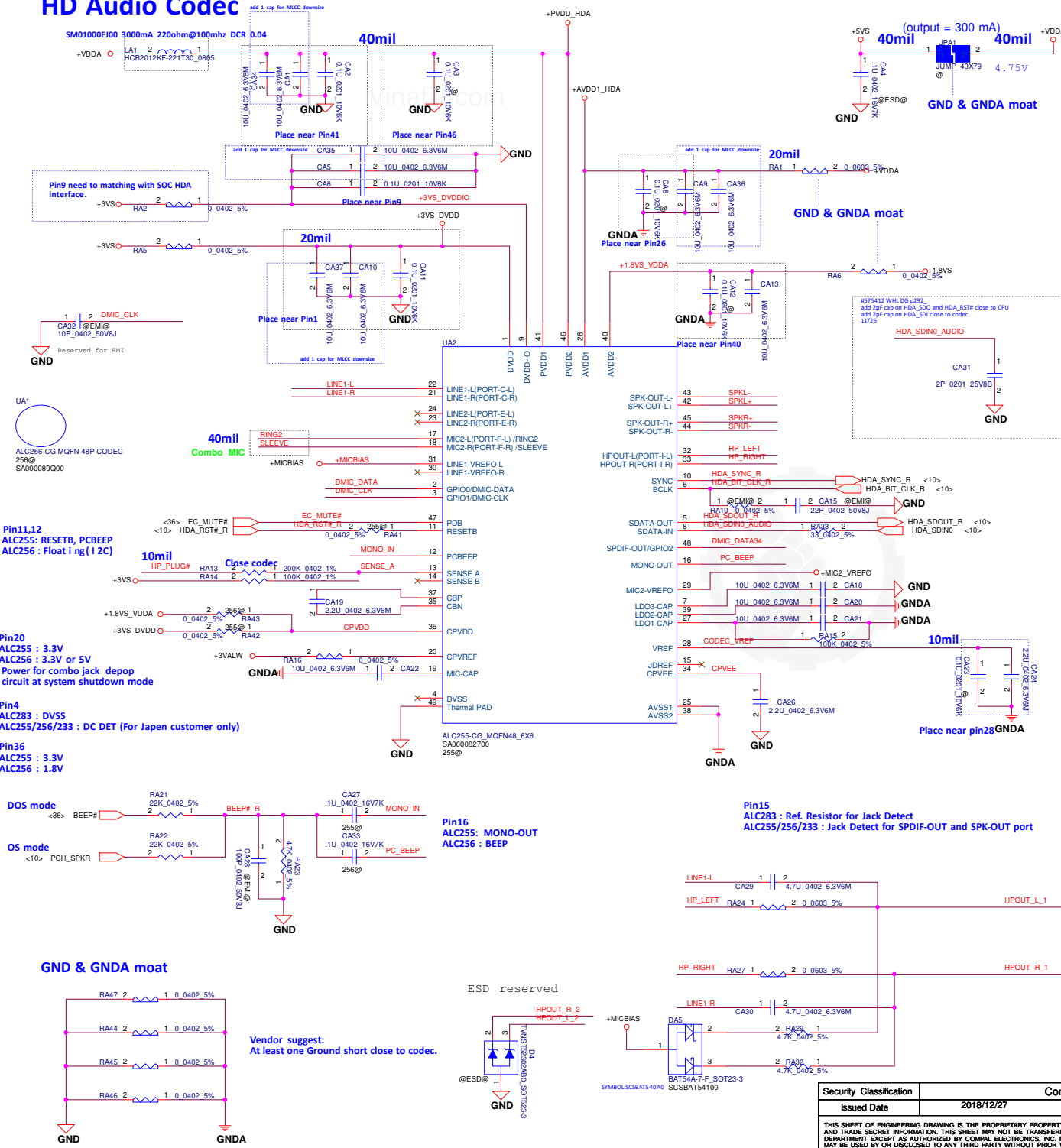
Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

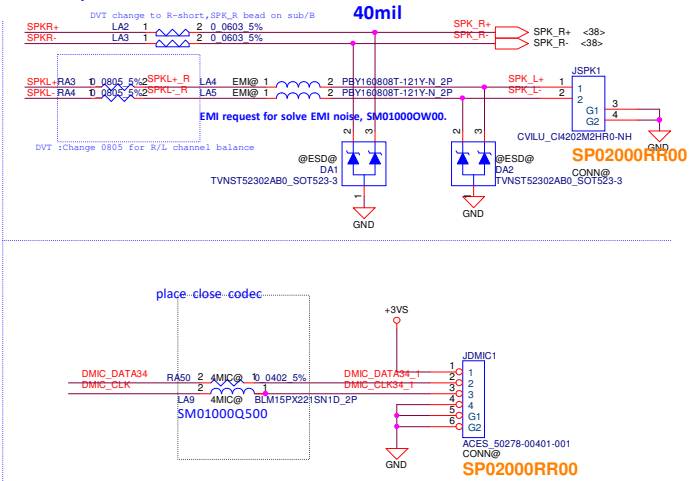


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					Size	Document Number		Rev.
					Custom	EH7LW M/B LA-H792P		0.
					Date:	Thursday, June 06, 2019	Sheet	24 of 46

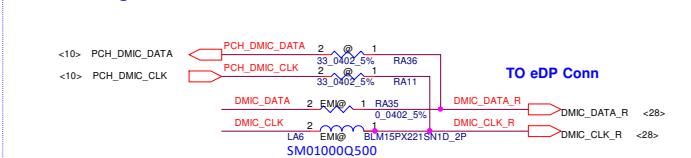
HD Audio Codec



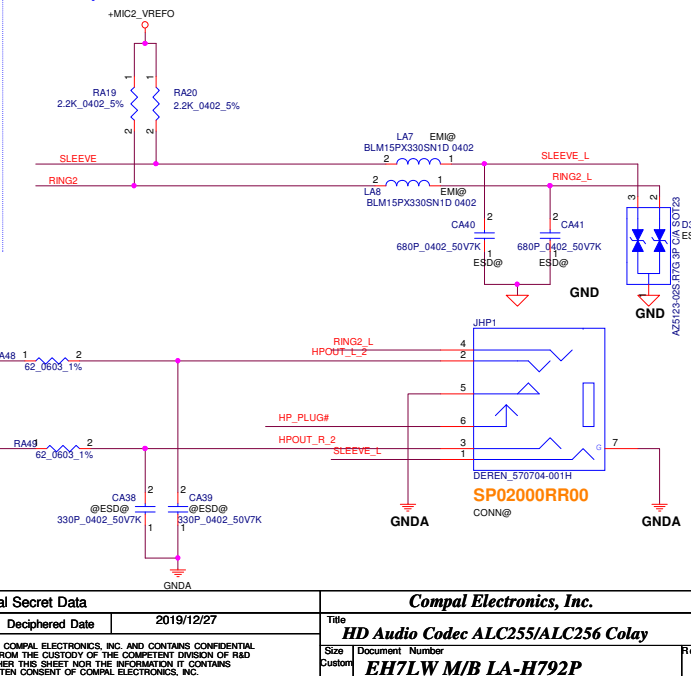
Int. Speaker Conn.



Digital MIC

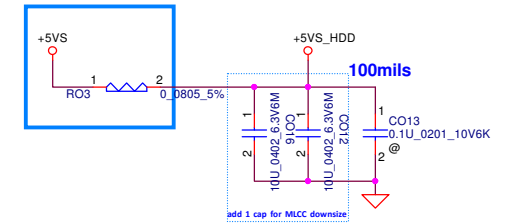
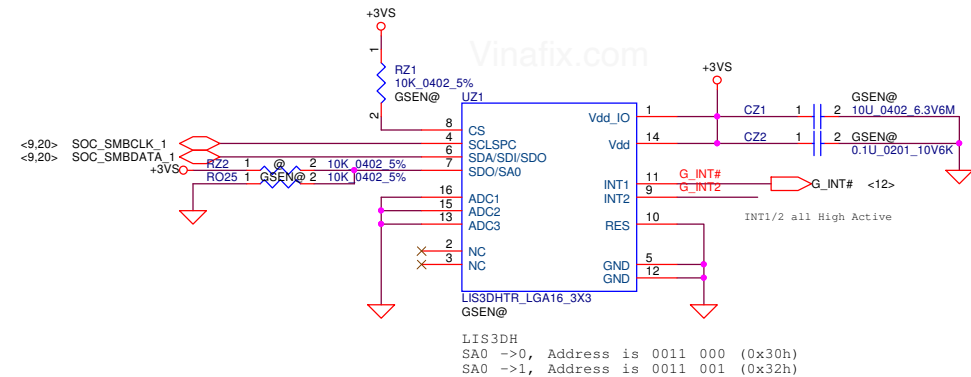


Headphone Out

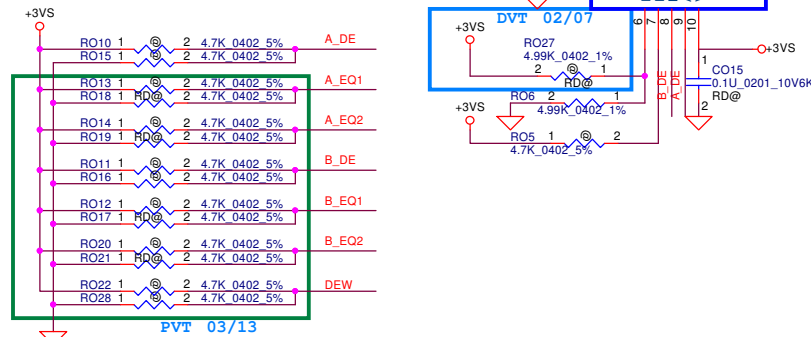
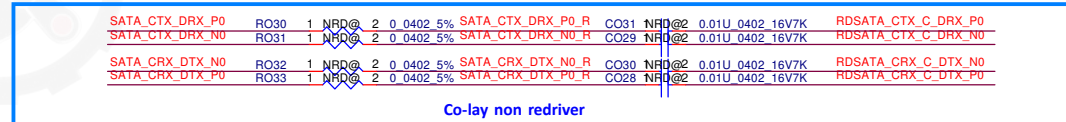
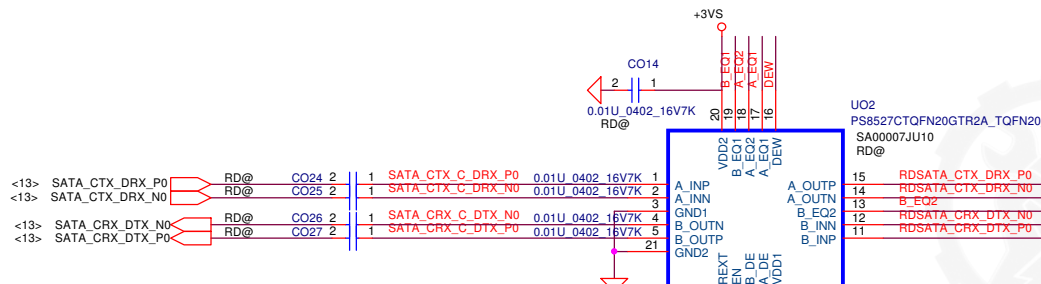
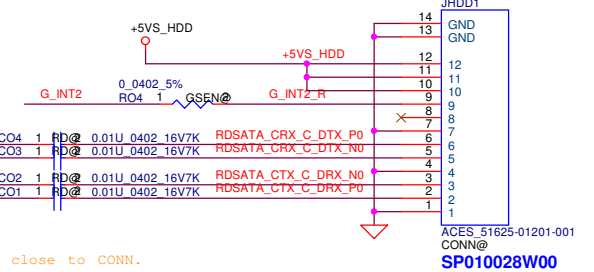


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				EH7LW MIB LA-H792P	0.1
				Date	Thursday, June 06, 2019
				Sheet	25 of 46

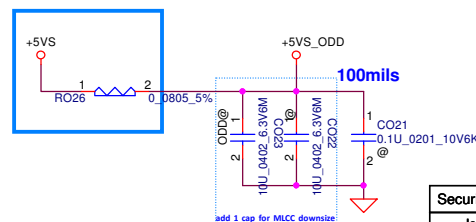
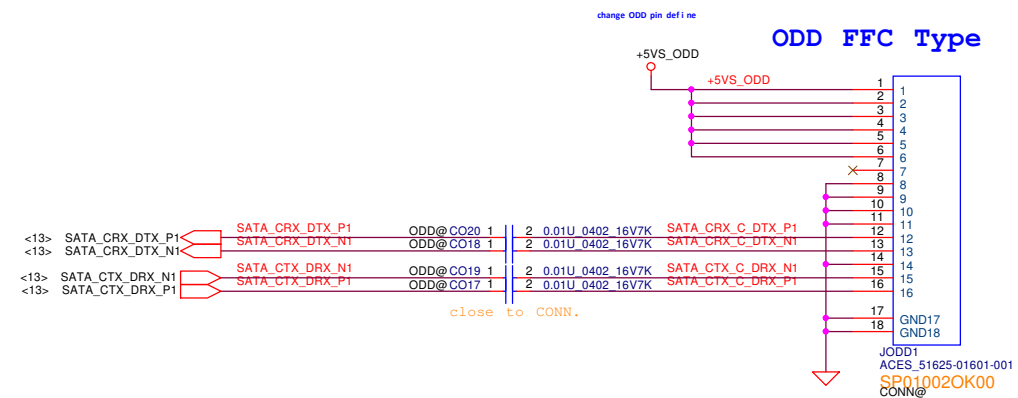
G-Sensor reserved for BA serial



HDD FFC Type



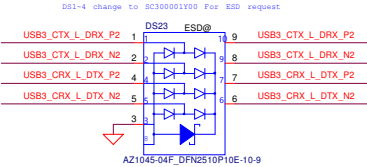
ODD FFC Type



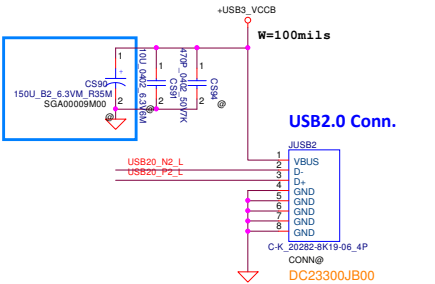
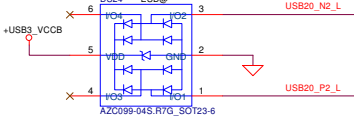
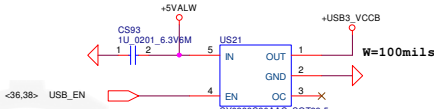
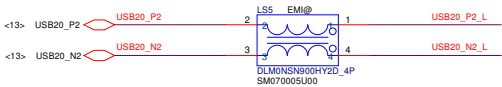
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Issued Date		2018/12/27		Deciphered Date		2019/12/27		Title		G-Sensor/HDD/ODD	
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								Custom		EH7LW M/B LA-H792P	
								Date:		Thursday, June 06, 2019	
								Sheet		26 of 46	
								Rev		0.1	

USB3.0 (Port 2)

USB port reserved



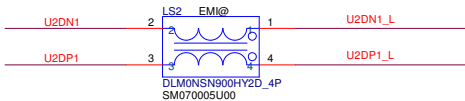
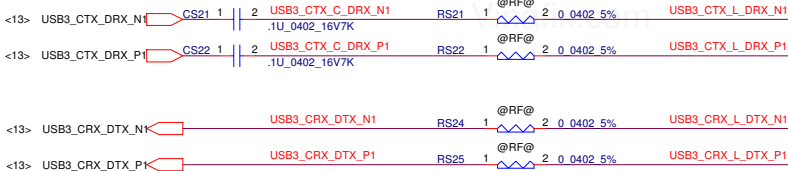
USB2.0 (Port 2)



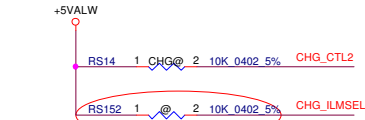
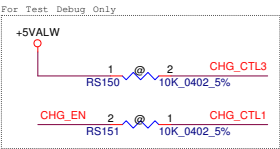
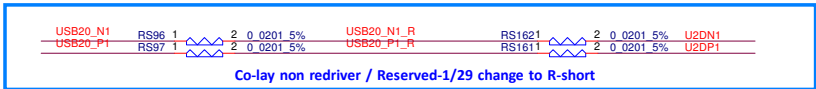
Symbol: DC23300N800
compatible: DC23300TT00

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USB3.0 (Port 1)



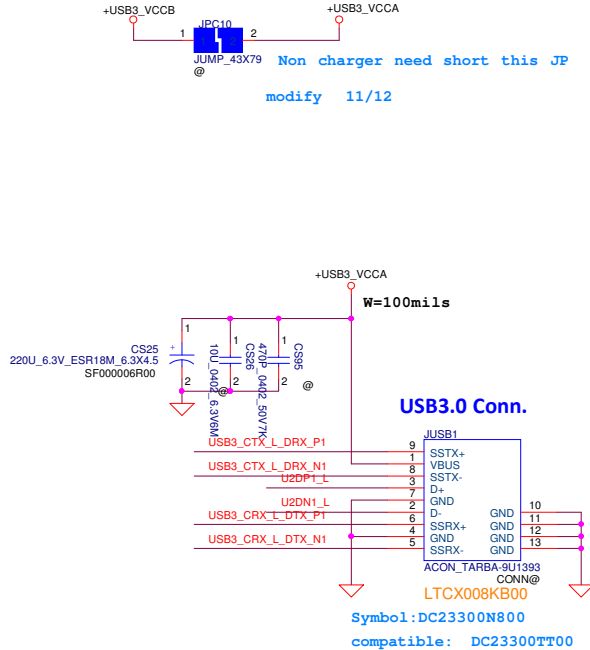
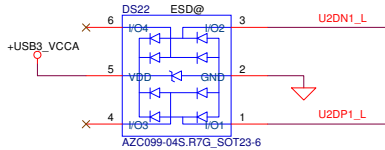
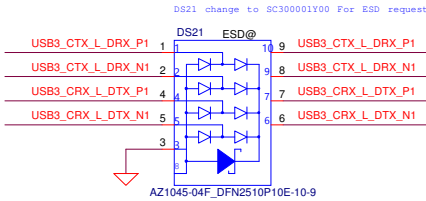
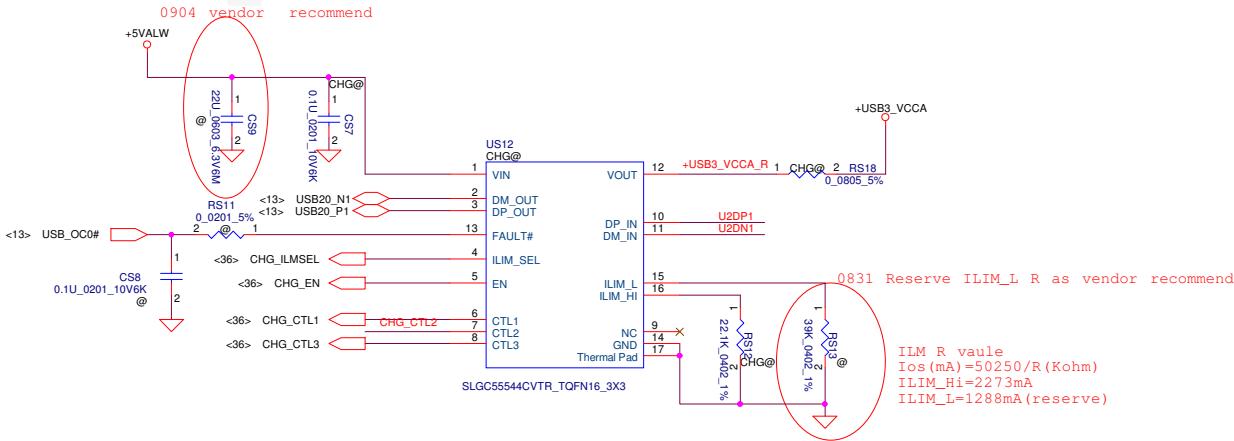
DVT: R-short

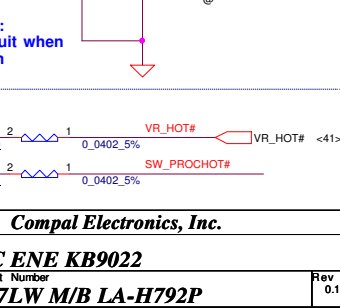
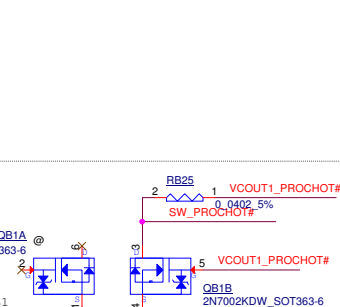
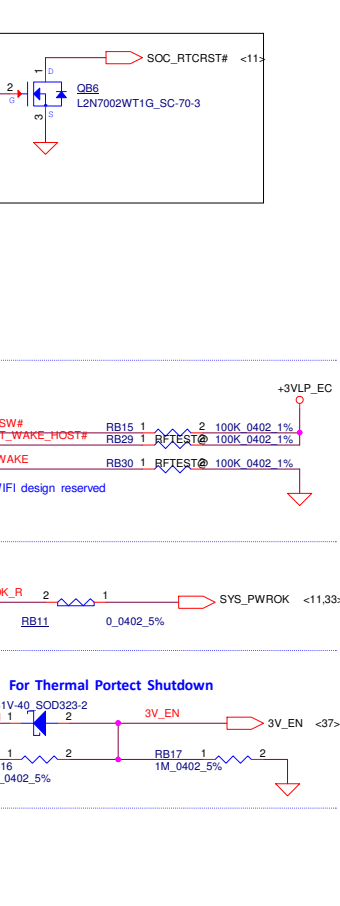
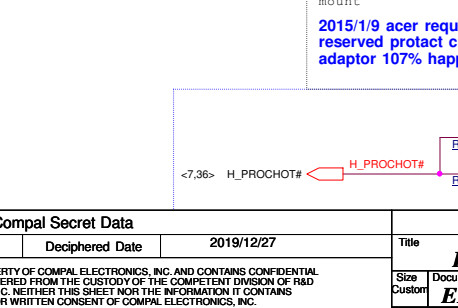
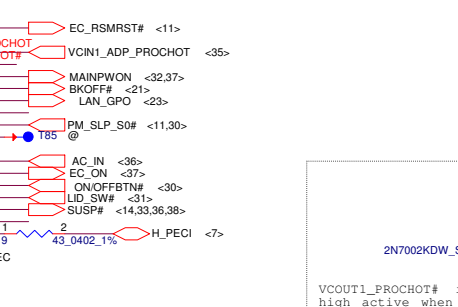
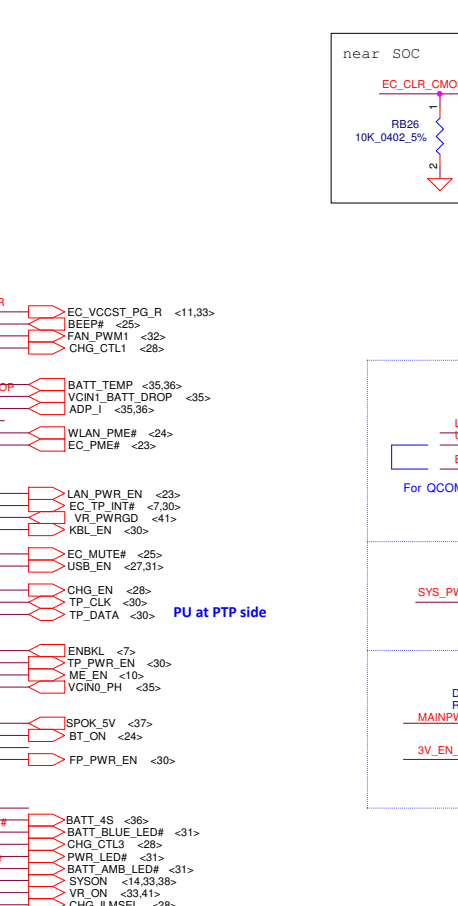
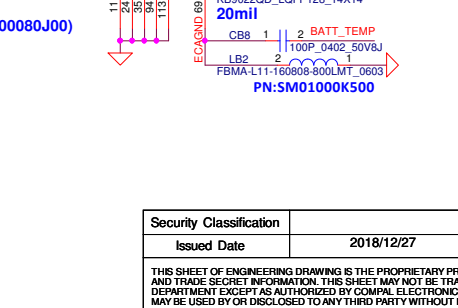
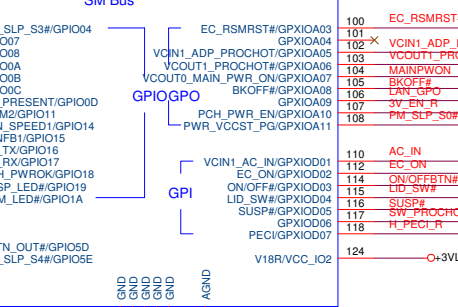
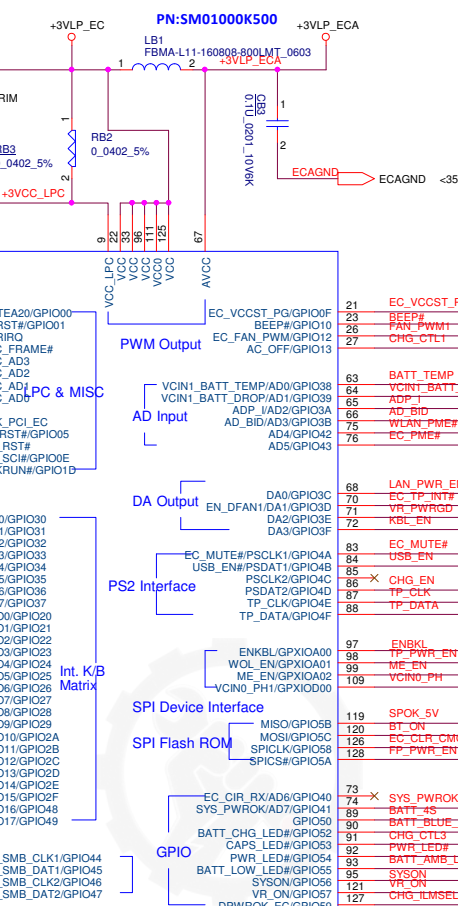
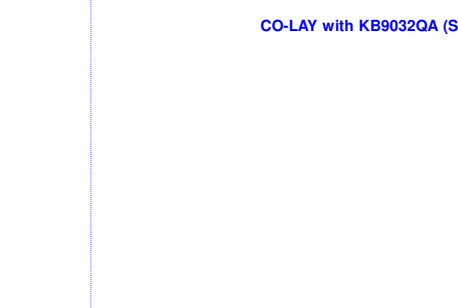
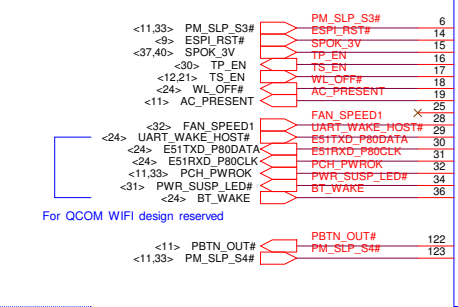
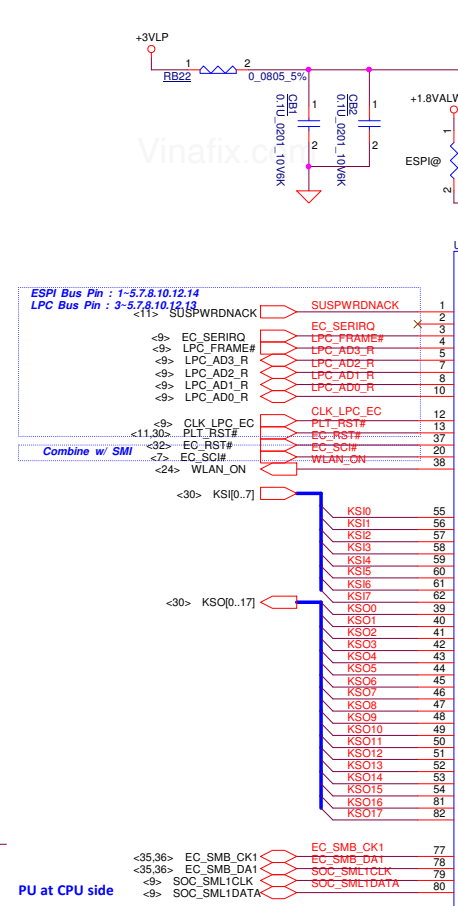
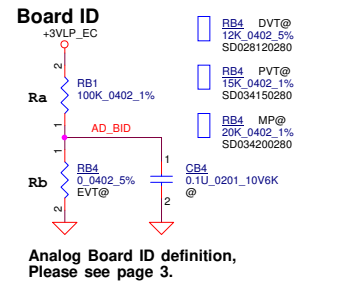
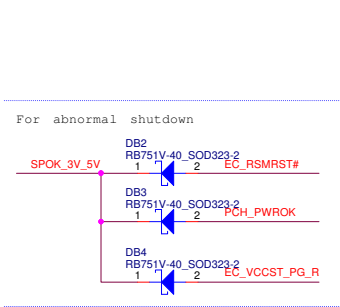
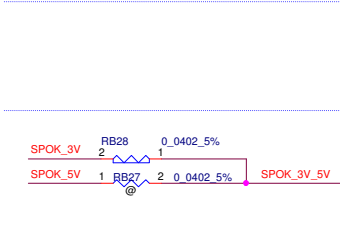
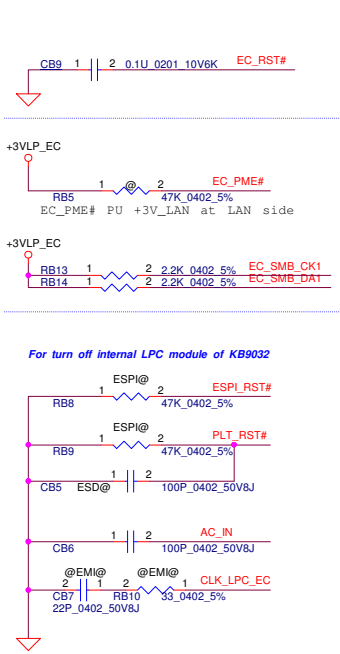


Rerserve PU, vendor suggest to EC control
if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected





For turn off internal LPC module of KB9032

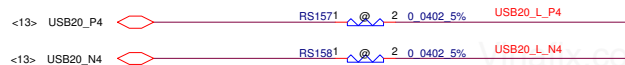
For abnormal shutdown

For QCOM WIFI design reserved

For Thermal Portect Shutdown

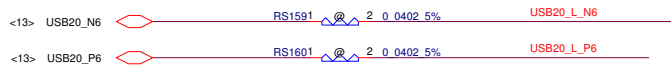
For QCOM WIFI design reserved

USB I/O



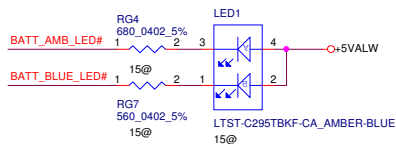
Card reader

Reserved CMC on SUB/B side

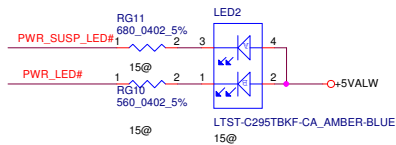


LED for 15" UMA

Battery LED



Power LED

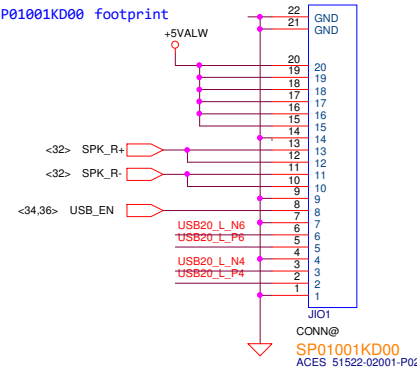


LID for 15" DIS

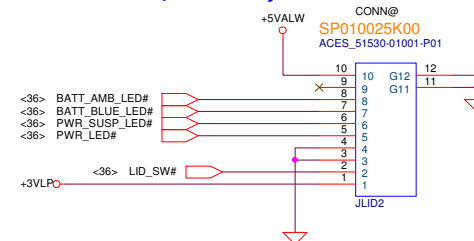
MB LID SW remove on UMA SKU

I/O Borad (USB2 /Card reader/ Speaker-RCH)

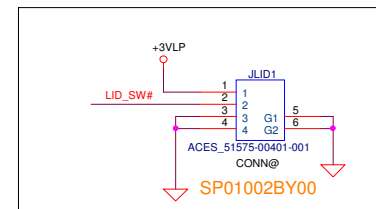
PVT:change to SP01001KD00 footprint



LID/B with LED for 17" UMA & DIS

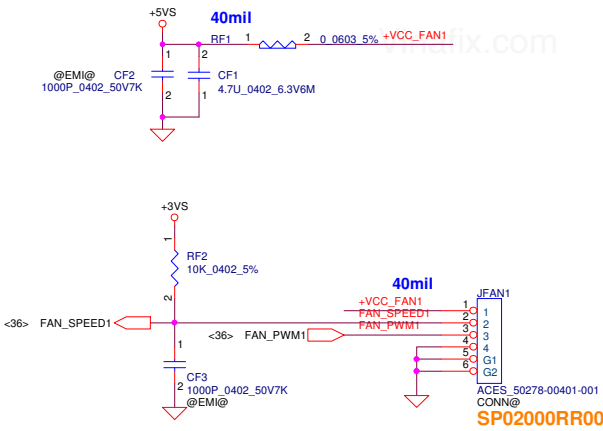


LID/B for 15" UMA 4pin

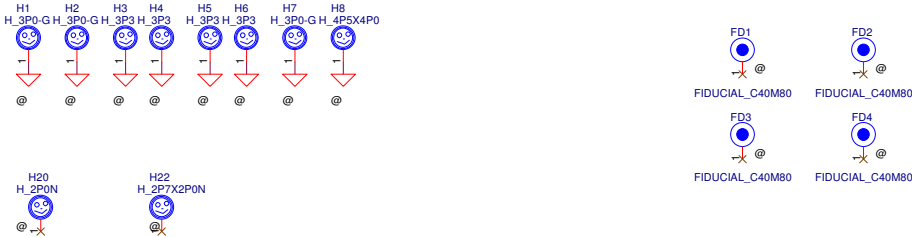


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2019/12/27				Title				IO/LID/LED			
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Date:				Thursday, June 06, 2019				Sheet			
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Rev				0.1				EH7LW M/B LA-H792P			

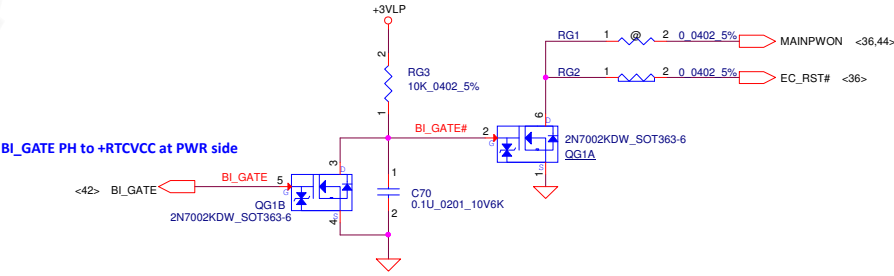
FAN1 Conn



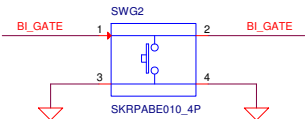
Screw Hole



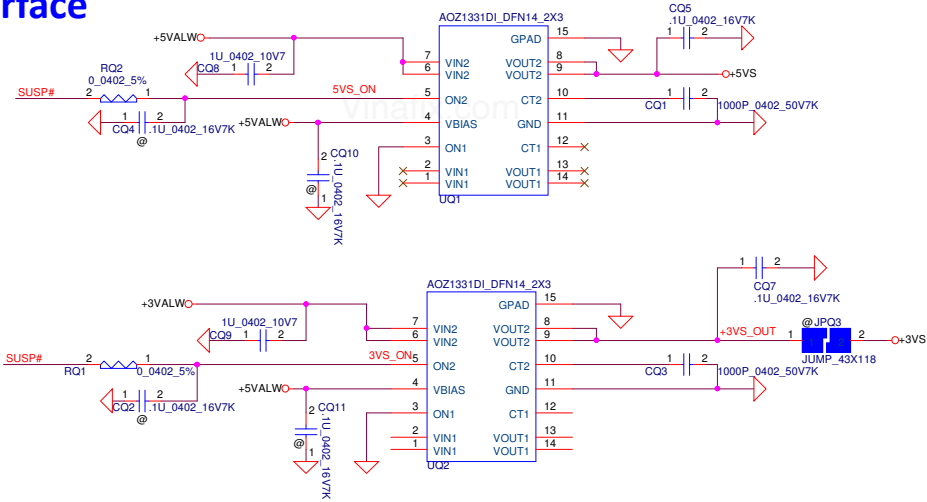
Reset Circuit



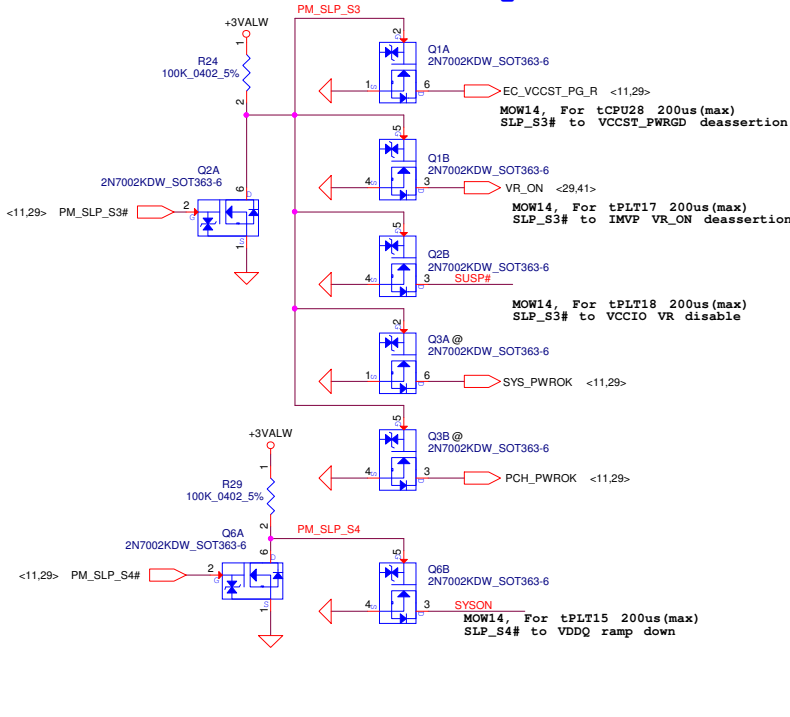
Reset Button



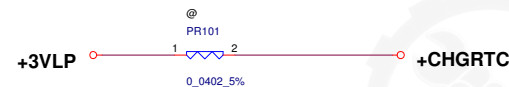
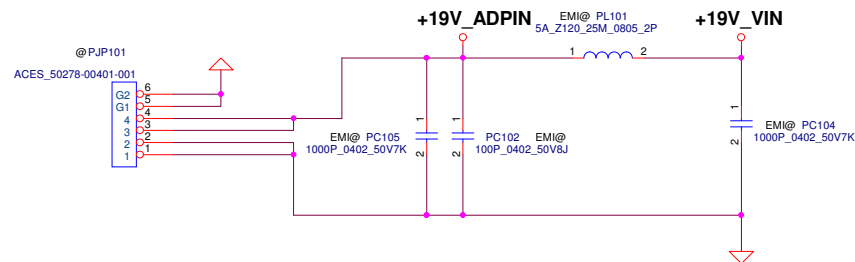
DC Interface



For Power ON/Off Sequence



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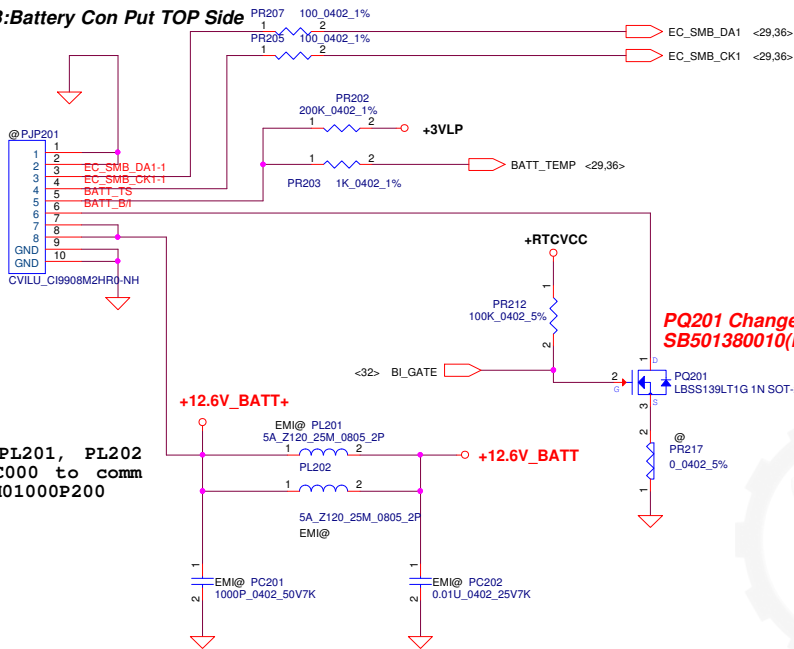


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MB:Battery Con Put TOP Side

Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



change PL201, PL202
SM01000C000 to comm
part SM01000P200

PQ201 Change to SB00000Q000,
SB501380010(BSS138LT1G Del)

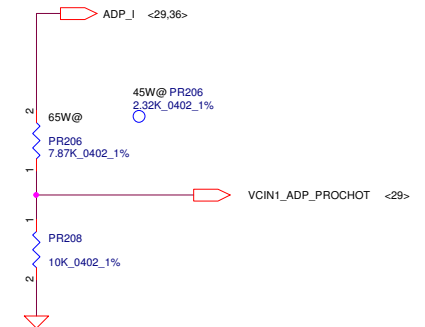
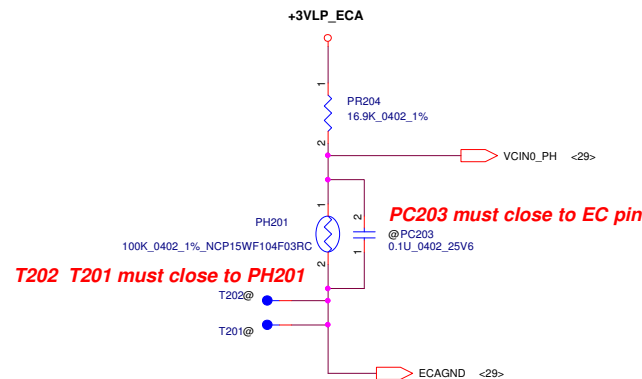
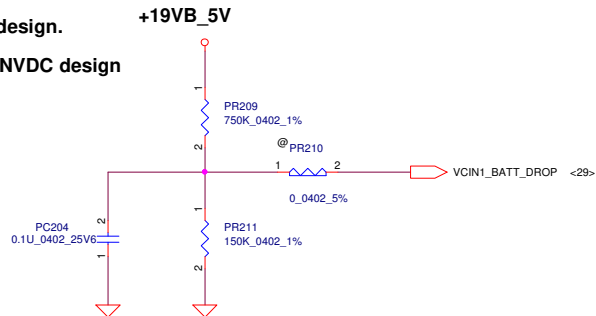
2016/11/16 update

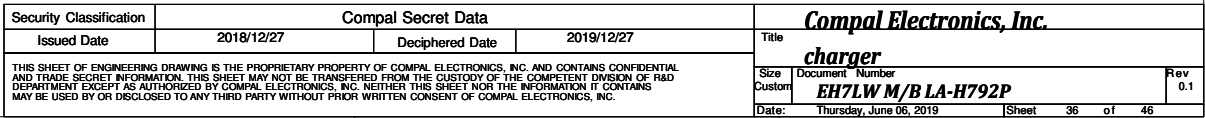
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 2.32K ohm	58.5W, 1V	Active=recovery
65W PR206 7.87K ohm	84.5W, 1V	Active=recovery
90W PR20K ohm	__W, __V	Active=recovery
PH1	2V	1V

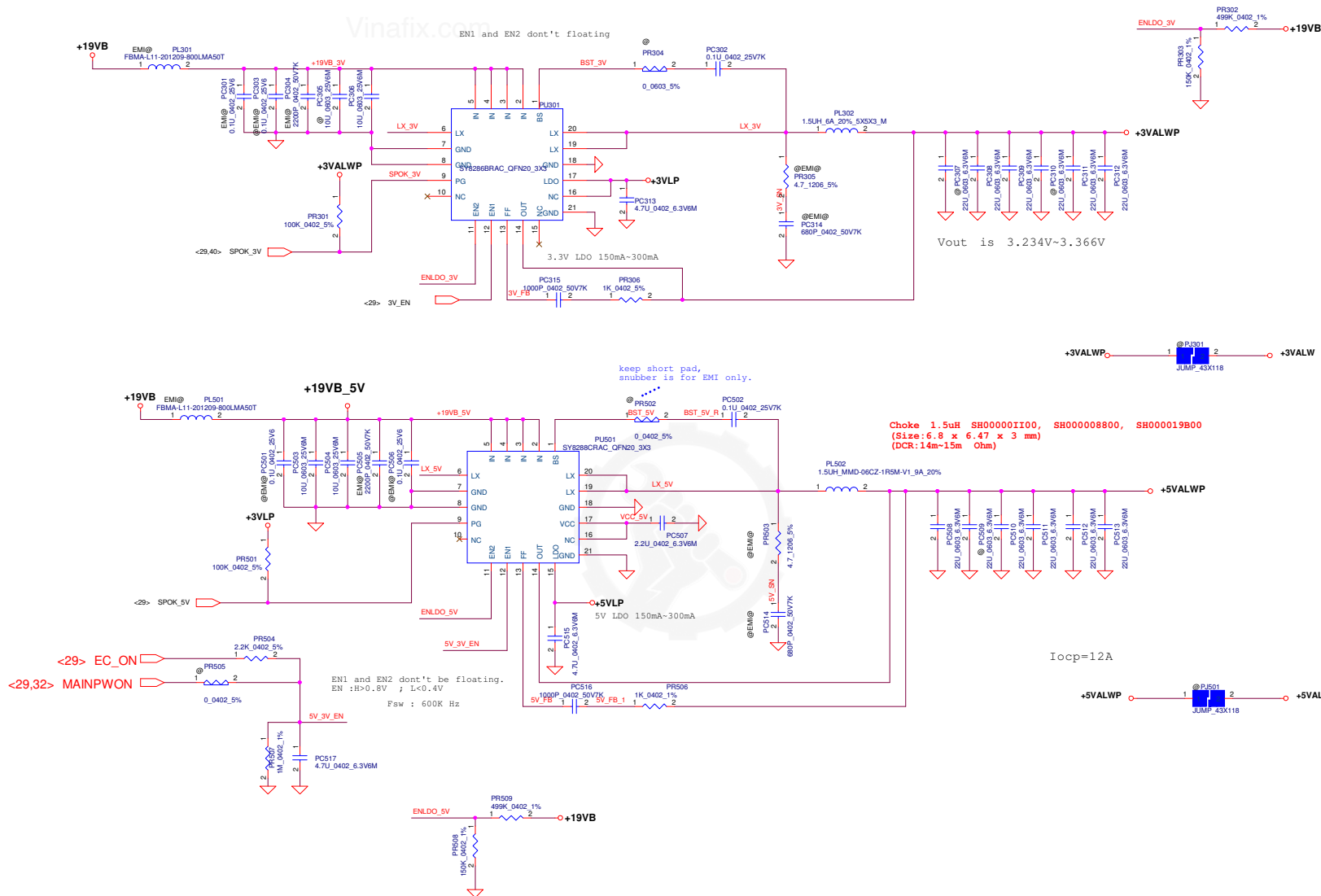
PH1 under CPU bottom side :
CPU thermal protection at 89 +3 degree C
Recovery at 56 +3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V







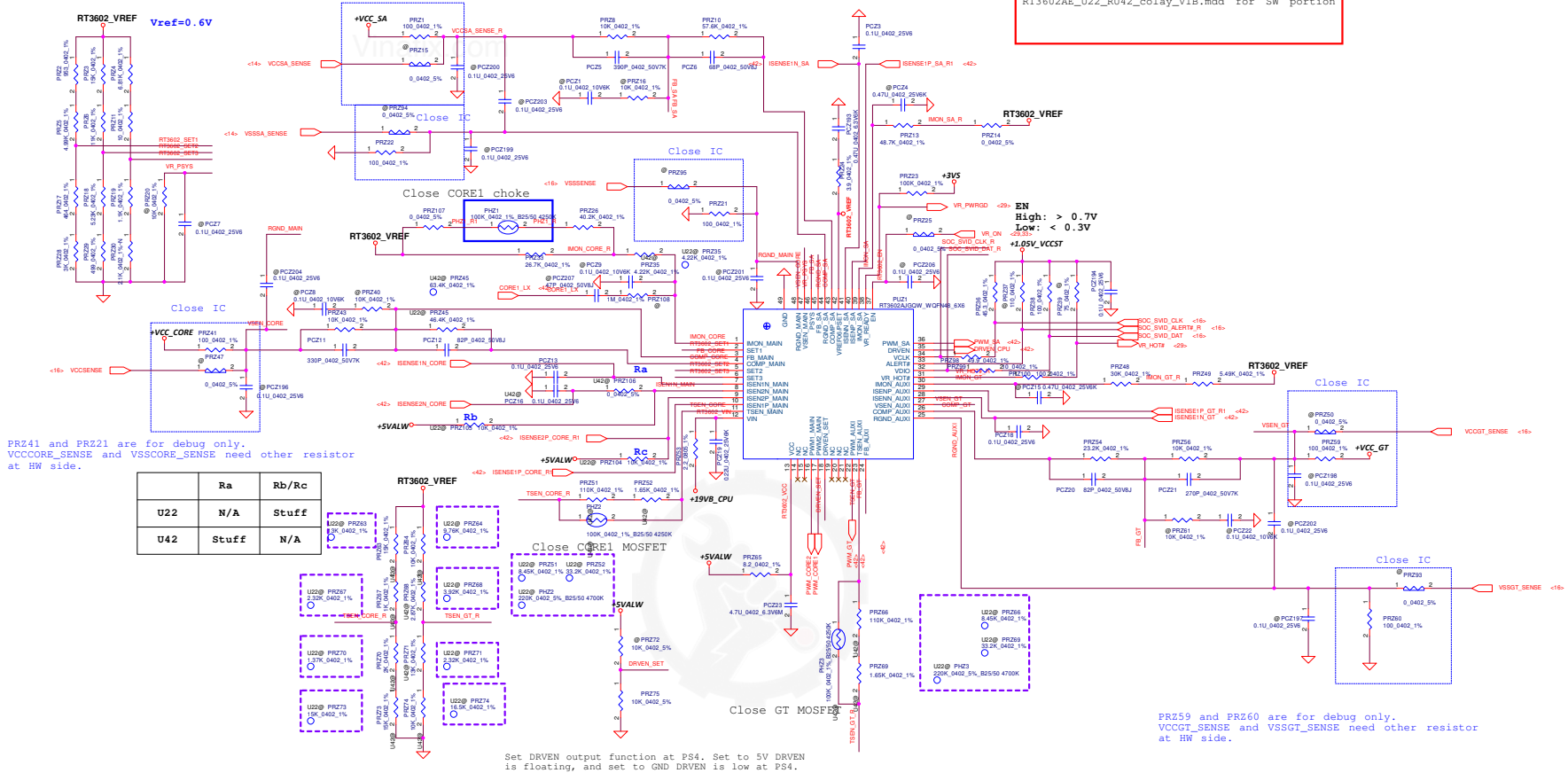
Security Classification		Compal Secret Data		Compal Electronics, Inc. VCCP	
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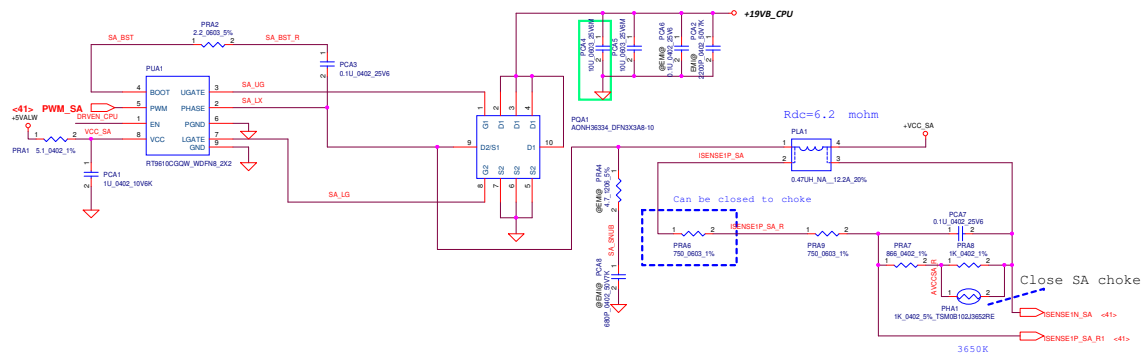
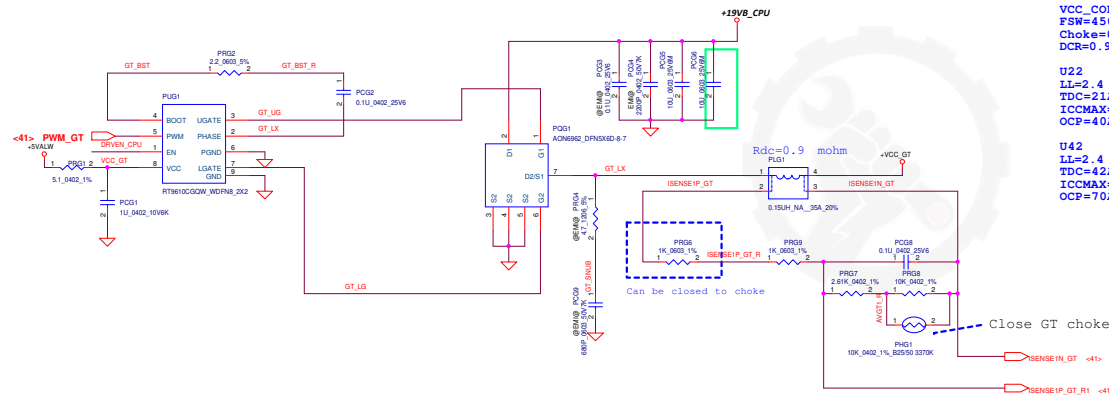
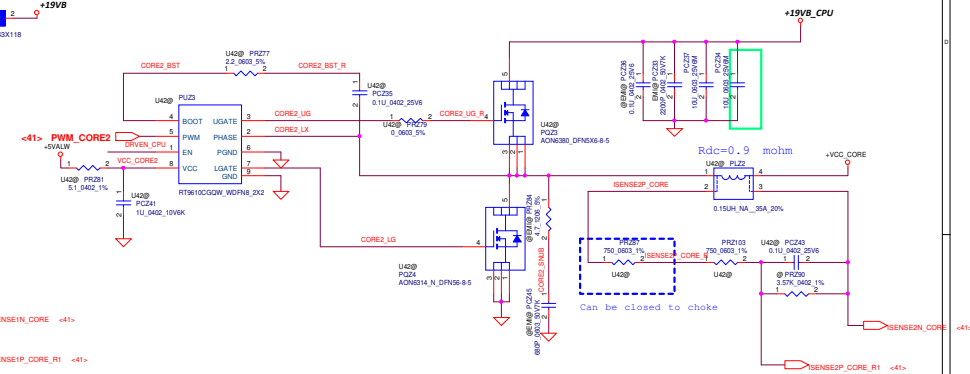
Module model information

RT3602AE_U22_RU42_colay_V1A.mdd for IC portion
RT3602AE_U22_RU42_colay_V1B.mdd for SW portion

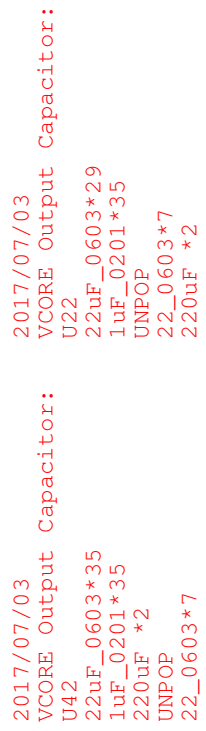
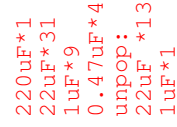
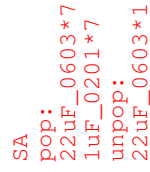
Close IC

PRZ1 and PRZ22 are for debug only.
VCCSSA_SENSE and VSSSA_SENSE need other resistor at HW side.





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				E7H7M/LB/M/BA-H7929	3.1
Date: 12/29/2019, 4:06:33 PM				Sheet	42 of 42



HW Schematic chang list (P.I.R)

Date	Rev.	Modify Item	Date	Rev.	Modify Item
1/22	0.1	Add cnvi cap(CM4) as intel request update JI01/JFP1 pin define Add UART routing for RF test			
1/29	0.1	update JI01 pin define change 0-ohm to R-short remove SWK1/UG1/UG2/JPQ2			
2/12	0.1	change RA3/RA4 to 0805 size			
3/13	1.0	Add DA3/DA4 for audio ESD protection			
3/15	1.0	change JI01 footprint update UL2 pin28/pin29 pin define Delete JC1 ROM socket change 0-ohm to R-short			
5/9	1A	update RC262 75k for CML			

HW Schematic chang list (P.I.R)

Item Page Date Rev. Reason for change Modify Item

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				Rev	0.1

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	change PL502 to common part	change PL502 to common part		P.44	change PL502 to common part(SH000016700)	19.0212	DVT
02							
03	change CAP size to 0402	change CAP size to 0402 for cost down		P.43,44	change PC302,PC502,PCB11 to SE00000W210 change PCB1 to SE074102K80	19.0212	DVT
	change 0 ohm to R-short	change 0 ohm to R-short for cost down			change PR101,PR217,PR210,PRB15,PRB17,PRB23,PRB26,PRB16,PR304,PR505,PR502,PRM8,PRM11,PRM12,PRF3,PRF8,PRF1,PR1801,PRZ15,PRZ94,PRZ47,PRZ95,PRZ50,PRZ93,PRZ25 to R-short (25PCS)	19.0212	DVT
04	DDR sequence	change PRM8 to 48.7K and PCM18 to 0.1u for sequence		P.38	change PRM8 to SD034487280 change PCM18 to SE102104K00	19.0215	DVT
05	CPU transient	change R and C value for CPU transient test		P.48	change PCZ11 to 330PuF(SE074331K80) change PRZ45 to 63.4k ohm(SD03463K280)(U42) change PRZ49 to 5.49k ohm(SD034549180)	19.0218	DVT
06	DDR sequence	change PRM8 to 0 ohm and del PCM18 for sequence		P.38	change PRM8 to SD028000080 del PCM18	19.0328	PVT
07	VR thermal alert adjust	change protect from 100c to 110c		P.41	change PHZ2,PHZ3 to SL200002I00, change PRZ51,PRZ66 to SD000000680, change PRZ52,PRZ69 to SD034332280, change PRZ67 to SD00000WS80,change PRZ63 to SD034130280, change PRZ70 to SD034137180,change PRZ68 to SD034392180, change PRZ64 to SD034976180,change PRZ71 to SD00000WS80,change PRZ74 to SD034165280	19.0507	pre MP
08							
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